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Comparative analysis of dc boost voltage source inverter and z-source inverter

MOHIT TYAGI[1], ATUL KUSHWAHA[2], ALOK TYAGI[3]

Asst.Prof, Electrical And Electronics Engineering, Vidya College of Engineering Meerut[1]

Asst.Prof, Electrical And Electronics Engineering, IMS Engineering College Ghaziabad[2]

Asst.Prof, Electrical And Electronics Engineering, RKGIT Ghaziabad[3]

Abstract : This paper aims to analyse the performances of both the dc boost VSl and the Z-source inverter. The algorithm to control linearly the capacitor voltage is suggested in order to improve the transient response for dc boost control of the Z-source inverter. The peak ac output voltage is used to control exactly the ac output voltage to its desired level.

Keywords: Z-source inverter, The dc boost VSl

INTRODUCTION

The boosted dc VSI converter consists of a boost converter and a voltage source inverter (VSI). The function of the boost converter is to boost the low input DC voltage V_{dc} to feed the VSI and the Dc-link voltage of the VSI is shown in figure1

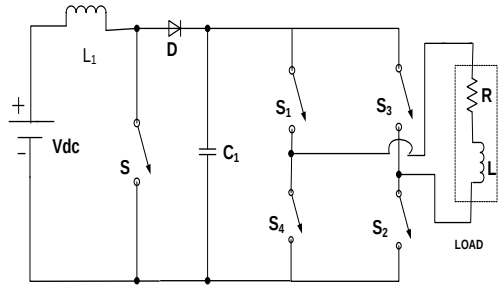

Figure 1 Boosted DC VSI Converter

The boost L is selected based on the maximum-allowed ripple current (ΔI) at maximum duty cycle (D) at the peak minimum line voltage [V_{in}(min)] and minimum output voltage [V_{out}(min)]. The following equations were used to calculate the required inductor for the boost power stage for a prototype power supply. A decrease in maximum duty cycle, causing the boost inductor to decrease,

$$D = 1 - \frac{V_{in}(\min) * \sqrt{2}}{V_{out}(min)}$$

$$L = \frac{V_{in}(min) * \sqrt{2} * D}{\Delta I * f_s}$$

$$\Delta I = \frac{P_{out} * \sqrt{2} * 0.2}{V_{in}(min)}$$

The dc link capacitor decouples the VSI and boost converter and keep dc link voltage ripple to an adequate level. A feasible power flow control method could be to keep the dc link voltage constant via the boost converter.

Z-source inverter outputs a required voltage by adjusting the shoot through duty ratio with the restriction to keep the voltage across the switches not to exceed the limits . The Z-source inverter has one switch less than the DC/DC boosted PWM inverter but the DC/DC boosted PWM inverter has better efficiency at low loads .

The Z-source converter (ZSC) is a new topology in power conversion, which has unique features that can overcome the limitations of VSI and CSI . Figure 2.shows the ZSC implemented as a single phase DC/AC converter (inverter). Although DC/AC conversion is the most common application of the Z-source topology, it can also be applied to AC/DC and AC/AC power conversions . The X shape impedance is the Z-source network which is composed of two split inductors and two capacitors to provide a coupling between the DC source and the inverter bridge. The Z-source inverter (ZSI) has the unique buck-boost capability which ideally gives an output voltage range from zero to infinity regardless of the input voltage. This is achieved by using a switching state that is not permit in the VSI which is called the —"shoot-through" state. This is the state when both upper and lower switches of a phase leg are turned on. In a conventional VSI switching pattern, there are eight permissible switching states. Six of those switching states are called the —"active" states where the load sees the input voltage and the remaining two states are called the —"zero" states here ither all the upper or all the lower switches are on and the load sees zero voltage.

Figure 3(a) shows the carrier based PWM switching pattern for a VSI. According to this switching method, the reference signals for the three phase voltages are compared to a triangular carrier signal. If a reference signal is greater than the carrier signal, the upper switch in the leg of the corresponding phase becomes on and the lower switch of the same phase leg becomes off and vice

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versa. All of the 8 permissible switching states of a VSI can be distinguished from Figure. 3(a) including the two zero states. First zero state occurs when the carrier wave is greater than all of the reference signals, i.e. all the upper leg switches are on and the lower leg switches are off. The second zero state occurs when the carrier wave is smaller than all of the reference signals.

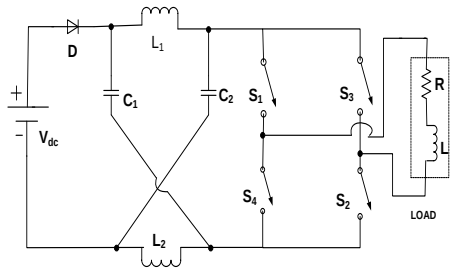


Figure .2 ZSC implemented as single-phase inverter (ZSI)

The shoot-through state can be distributed among the carrier based switching pattern of the VSI in Figure 3(a). without distorting the carrier based PWM signal generation. Figure 3 (b) illustrates the addition of the shoot-through state as equally distributed amounts of time inside the zero states. It can be seen from Figure 3(b) that the active states for both carrier based PWMs are the same for the VSI and the ZSI. This guarantees that the modulation index () which is defined as M the ratio of the total active states to the whole period, is the same for both switching patterns.

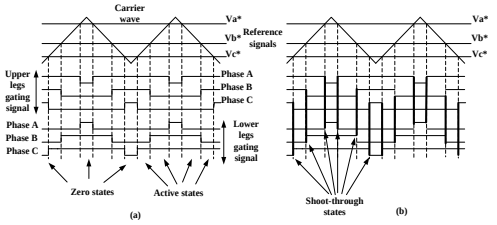


Figure 3 (a) carrier based PWM (b) Modified carrier based PWM for ZSI

MATHEMATICAL MODEL OF BOOST CONVERTER

The operation of boost converter can be divided into two modes. Mode 1 begins when switch M1 is switched on at t = 0. The input current, which rises, flow through inductor L and switch M1. Mode 2 begins when switch M1 is switched off at t = t_1. The current that flowing through the switch would now flow through L, C, load, and diode D_m. the inductor current falls until switch M1 is turned on again in the next cycle. The energy stored in inductor L is transferred to the load. The equivalent circuits for the modes of operation are shown in figure. The waveforms for voltages and currents are shown in figure for continuous load current, assuming that the current rises or falls linearly.

Assuming that the inductor current rises linearly from I_1 to I_2in the time t_1,

$$V_s = L\frac{I_2 - I_1}{t_1} = L\frac{\Delta I}{t_1} \quad \ldots. (2.1)$$

Or

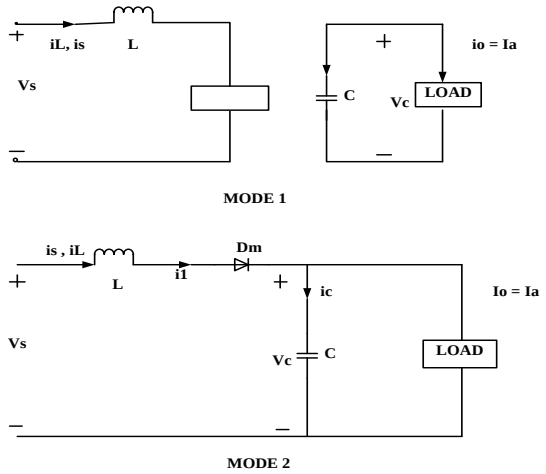
$$t_1 = \frac{\Delta IL}{V_s} \quad \ldots. (2.2)$$

And the inductor current falls linearly from I_2 to I_1 in time t_2,

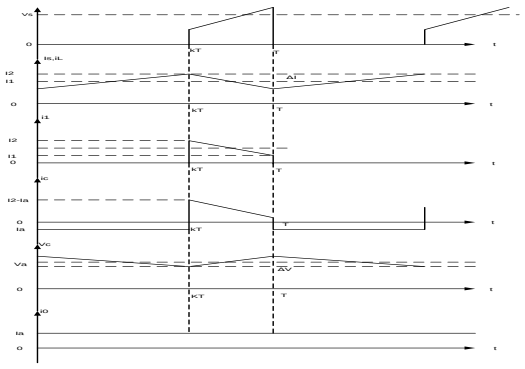
$$V_s - V_a = -L\frac{\Delta I}{t_2} \quad \ldots\ldots..(2.3)$$

or

$$t_2 = \frac{\Delta IL}{V_a - V_s} \quad \ldots. (2.4)$$



(a) Equivalent Circuits



(b) Waveforms

Figure 4. Boost Regulator with continuous i_L.

Where $\Delta I = I_2 - I_1$is the peak-to-peak ripple current of inductor L. From Eqs (3.1) and (3.3),

$$\Delta I = \frac{V_s t_1}{L} = \frac{(V_a - V_s)t_2}{L} \quad \ldots. (2.5)$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$ yields the average output voltage,

$$V_a = V_s\frac{T}{t_2} = \frac{V_s}{1-k} \quad \ldots. (2.6)$$

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Which gives

$(1–k)=\frac{V_s}{V_a}$ …. (2.7)

Substituting $k = t_1/T = t_1 f$ into Eq (3.7) yields

$t_1 = \frac{V_a - V_s}{V_a f}$ …. (2.8)

Assuming a lossless circuit, $V_s I_s = V_a I_a = V_s I_a/(1- k)$ and the average input current is

$I_s = \frac{I_a}{1-k}$ ….(2.9)

The switching period T can be found from

$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta IL}{V_s} + \frac{\Delta IL}{V_a - V_s} = \frac{\Delta ILV_a}{V_s(V_a - V_s)}$ …. (2.10)

and this gives the peak-to-peak ripple current:

$\Delta I = \frac{V_s(V_a - V_s)}{fLV_a}$ …. (2.11)

or

$\Delta I = \frac{V_s k}{fL}$ …. (2.12)

When the transistor is on, the capacitor supplies the load current for $t = t_1$. The average capacitor current during time t_1 is $I_c = I_a$ and the peak-to-peak ripple voltage of the capacitor is

$\Delta V_c = v_c - v_c(t=0) = \frac{1}{C}\int_0^{t_1} I_c\, dt = \frac{1}{C}\int_0^{t_1} I_a = \frac{I_a t_1}{C}$ … (2.13)

Substituting $t_1 = (V_a – V_s)/(V_s f)$ from Eq. (3.8) gives

$\Delta V_c = \frac{I_a(V_a - V_s)}{V_a f C}$ …. (2.14)

or

$\Delta V_c = \frac{I_a k}{fC}$ …. (2.15)

Condition for continuous inductor current and capacitor voltage. If I_L is the average inductor current, the inductor ripple current

$\Delta I = 2I_L$.

Using Eqs.(3.6) and (3.12), we get

$\frac{kV_s}{fL} = 2I_L = 2I_a = \frac{2V_S}{(1-k)R}$ …. (2.16)

which gives the critical value of the inductor L_C as

$L_C = L = \frac{k(1-k)R}{2f}$ …. (2.17)

If V_C is the average capacitor voltage, the capacitor ripple voltage $\Delta V_C = 2V_a$. Using Eq. (3.15), we get

$\frac{I_a k}{Cf} = 2V_a = 2I_a R$ …. (2.18)

which gives the critical value of the capacitor C_c as

$C_c = C = \frac{k}{2fR}$ …. (2.19)

A boost regulator can set up the output voltage without a transformer. Due to a single transistor, it has a high efficiency. The input current is continuous. However, a high-peak current has to flow through the power transistor. The output voltage is very sensitive to changes in duty cycle k and it might be difficult to stabilize the regulator. The average output current is less than the average inductor current by a factor of $(1 – k)$, and a much higher rms current would flow through the filter capacitor, resulting in the use of a longer filter capacitor and a larger inductor than those of a buck regulator.

MATHEMATICAL MODEL OF VOLTAGE SOURCE INVERTER

The output in various form can be obtained as follows.

(i) RMS Output Voltage

The average value of the output voltage is given by

$V_{o(av)} = \frac{1}{2\pi}\int_0^{2\pi} v_o(\omega t)\, d\omega t$

Now, rms value of the output voltage is given by

$V_{o(rms)} = \sqrt{\frac{1}{2\pi}\int_0^{\pi/2} v_o^2(\omega t) d\omega t} = \sqrt{\frac{2}{\pi}\int_0^{\pi/2} V_{dc}^2\, d\omega t} = V_{dc}$ …. (2.20)

RMS value of a square-wave is equal to its peak-value.

(ii) Instantaneous Output-Voltage

The fourier-series can be found out by using the following equation:

$v_o(\omega t) = \sum_{n=1,2,3,\ldots}^{\infty} C_n \sin(n\omega t + \Phi_n)$

where, $C_n = \sqrt{a_n^2 + b_n^2}$, and $\Phi_n = \tan^{-1}(a_n/b_n)$

and $a_n = \frac{1}{\pi}\int_0^{2\pi} v_o(\omega t).\cos(n\omega t)\, d\omega t = 0$, due to square-wave symmetry and

$b_n = \frac{1}{\pi}\int_0^{2\pi} v_o(\omega t).\sin(n\omega t)\, d\omega t$

Due to quarter-wave symmetry, $b_n = 0$, for all even ‘n’.

$b_n = \frac{4}{\pi}\int_0^{\pi/2} V_{dc}.\sin(n\omega t) d\omega t$, for all odd ‘n’.

$b_n = \frac{2V_{dc}}{n\pi}$, for odd value of n.

$\therefore C_n = \sqrt{a_n^2 + b_n^2} = \frac{2V_{dc}}{n\pi}$ and $\Phi_n = \tan^{-1}\left(\frac{a_n}{b_n}\right) = 0$

Therefore, the instantaneous output voltage of the voltage source inverter can be expressed in fourier-series form as

$v_o(\omega t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4}{\pi}.\frac{V_{dc}}{n}\sin(n\omega t)$ …. (3.21)

= 0, for n = 2, 4, …. (even values of n)

(iii) Fundamental output voltage,

$V_{o(fund)} = \frac{2\sqrt{2}}{\pi}.V_{dc}$ …. (2.22)

(iv) n^{th} harmonic voltage

$V_o(n) = \frac{V_{o(fund)}}{n}$ …. (2.23)

(v) Switch (Device) Voltage and Current Ratings

$V_{CEO(transistor)} \geq 2\frac{V_{dc}}{2} \geq V_{dc}$ …. (2.24)

The current waveform for switch is a square-wave with peak vale of $V_{dc}/2R$

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$$\therefore I_{Tavg} = \frac{1}{T}\int_0^{T/2}\frac{V_{dc}}{R}dt = \frac{V_{dc}}{2R} \quad \ldots. \text{(2.25)}$$

$$\therefore I_{Trms} = \sqrt{\frac{1}{T}.\int_0^{T/2}\left(\frac{V_{dc}}{R}\right)2\,dt} = \frac{V_{dc}}{\sqrt{2}R} \quad \ldots. \text{(2.26)}$$

and

$$I_{Tpeak} = \frac{V_{dc}}{R} \quad \ldots. \text{(2.27)}$$

For square wave

$$V_O = V_{dc}[(S_1 \times S_2) - (S_3 \times S_4)] \quad \ldots. \text{(2.28)}$$

For UPWM

$$V_o = V_{dc}\sqrt{\frac{N_p.P}{\pi}} \quad \ldots. \text{(2.29)}$$

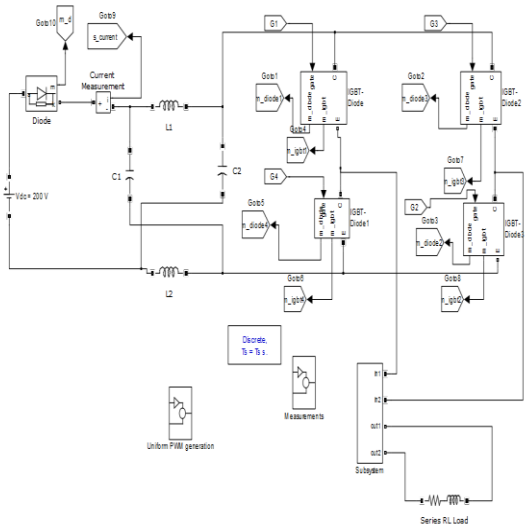
where,

N_p :- no. of pulses in half cycles.

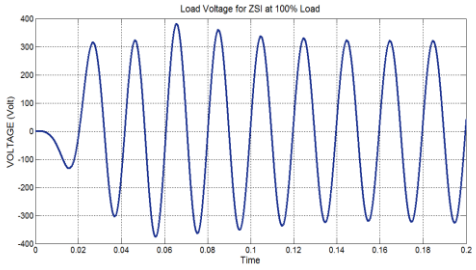
P :- duration of positive pulse.

Mathematical model of boosted VSI consists of two independent circuits, boost dc-dc converter and PWM based VSI. These well known mathematical models are studied to develop its simulink model.

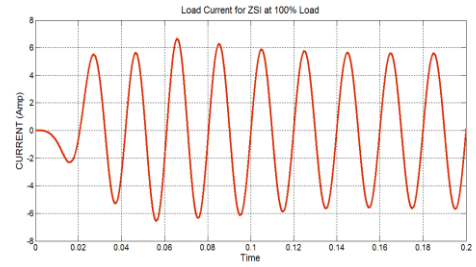
RESULTS AND DISCUSSIONS
OUTPUT RESULTS OF ZSI SIMULINK MODEL



The sinusoidal output voltage across load is shown in Figure 5(a) when ZSI is loaded for full load.Load current is shown in Figure 5(b) when ZSI is loaded for full load. Due to unexcited Z-network components, (L_1, L_2, C_1 and C_2) in the Z-source inverter achieved steady state at nearly 0.1 seconds. The boosting is clearly seen in the figures.



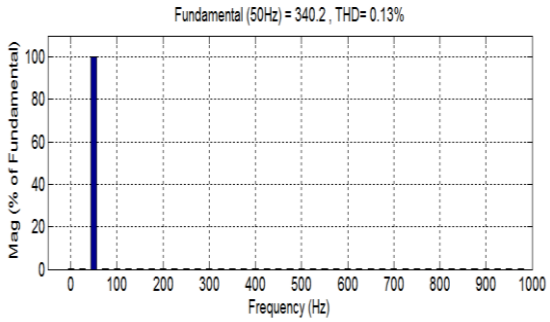
(a)



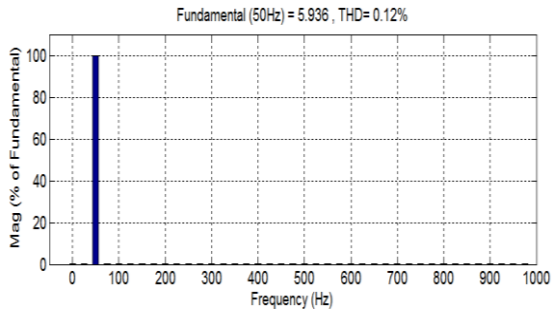
(b)

Figure 5(a) when ZSI is loaded for full load.Load current is shown in Figure 5(b) when ZSI is loaded for full load.

Fast Fourier Transform (FFT) analysis of output voltage and current at full load are shown in figure 6 less value of THD confirms the satisfactory performance of 1-Φ ZSI.



(a)



(b)

Figure 6 THD in (a) voltage (b) current for ZSI at full load

Figure 7 show the output voltage across and current through the load, when ZSI is loaded for 75% of the full load respectively.

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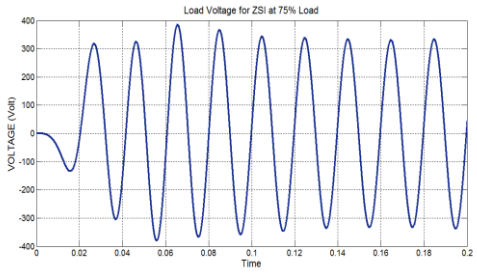

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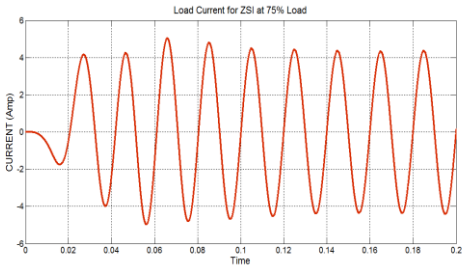
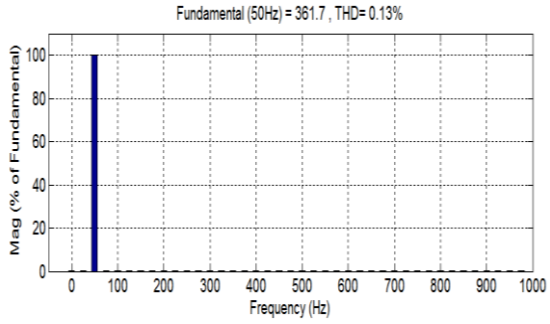


(b)

Figure 7 (a) voltage across (b) current through ZSI at 75% load

Fast Fourier Transform (FFT) analysis of output voltage and current at 75% load are shown in figure 8 less value of THD confirms the satisfactory performance of 1-Φ ZSI.



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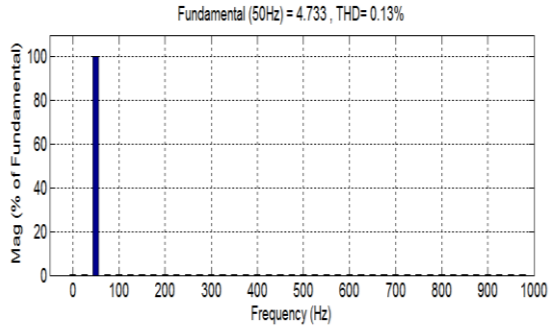
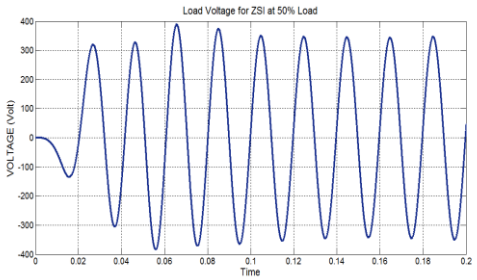


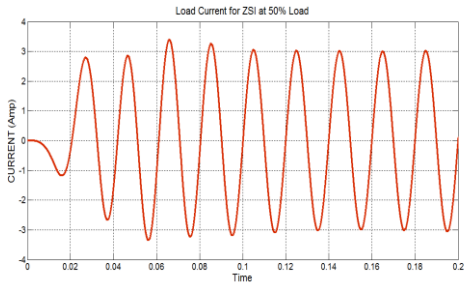
(b)

Figure 8 THD in (a) voltage (b) current for ZSI at 75% load

Output voltage across and current through the load, when ZSI is loaded for 50% of the full load respectively is shown below in figure 9



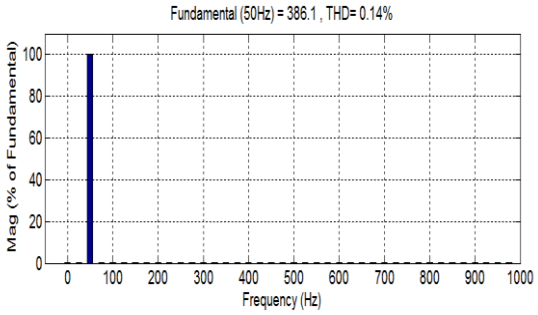
(a)



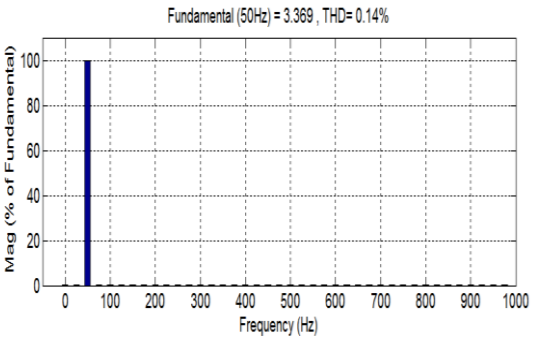
(b)

Figure 9 (a) voltage across (b) current through ZSI at 50% load

Fast Fourier Transform (FFT) analysis of output voltage and current at 50% load are shown in figure 10 less value of THD confirms the satisfactory performance of 1-Φ ZSI.



(a)



(b)

Figure 10 THD in (a) voltage (b) current for ZSI at 50% load

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Output voltage across and current through the load, when ZSI is loaded for 25% of the full load respectively is shown below in figure 11

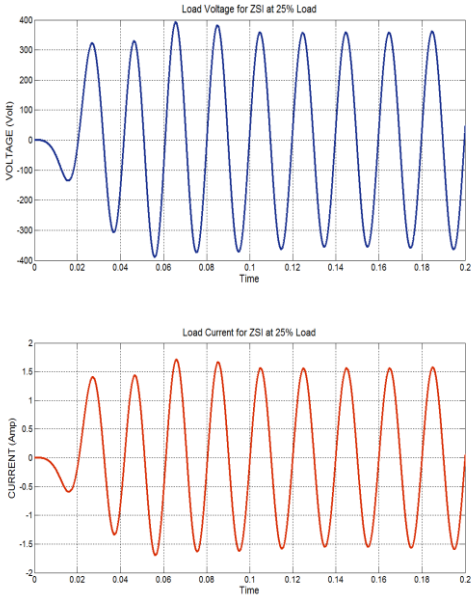
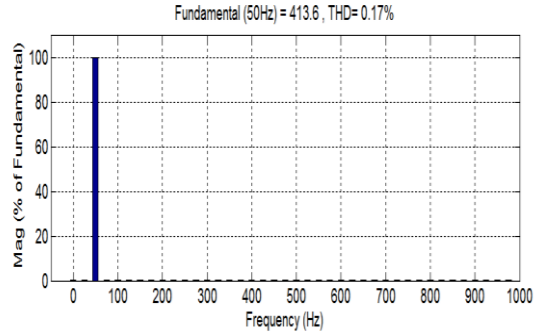
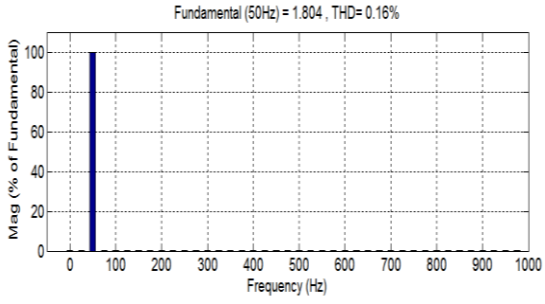


Figure11 (a) voltage across (b) current through ZSI at 25% load

Fast Fourier Transform (FFT) analysis of output voltage and current at 25% load are shown in figure 12 less value of THD confirms the satisfactory performance of 1-Φ ZSI.



(a)



(b)

Figure 12 THD in (a) voltage (b) current for ZSI at 25% load

Graphical presentation of output voltages when ZSI is loaded for 100%, 75%, 50% and 25% of full load is made in figure 6.9 which shows reduction in boosting with the increase in the load

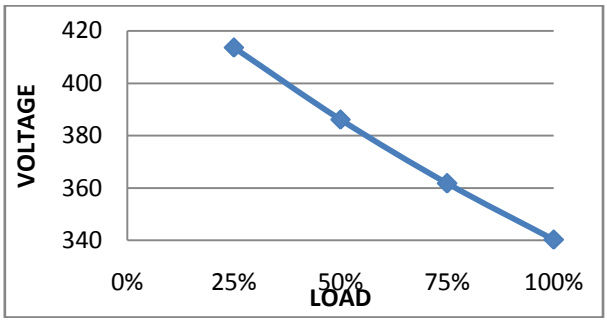


Figure 13 Variation in boosting voltage of ZSI

Figure 13 shows the graphically the variation in THD with respect to load. It is seen that THD decreases as the load increases.

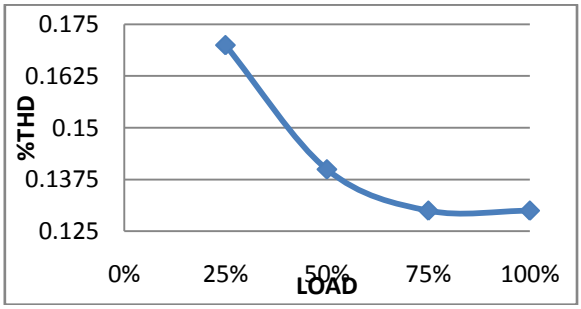


Figure 14 Variation in THD of ZSI

OUTPUT RESULTS OF BOOSTED DC VSI SIMULINK MODEL

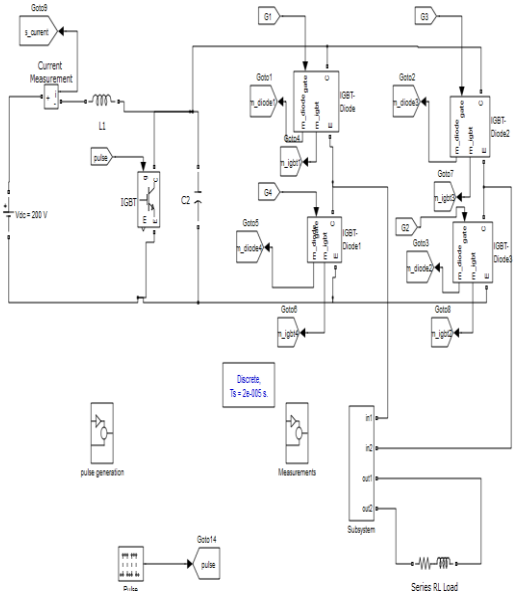


Figure 15 shows the output voltage across and current through load, when boosted dc VSI is loaded for full load.

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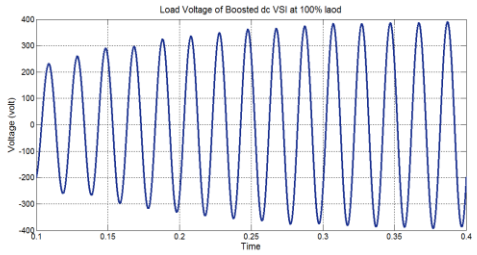
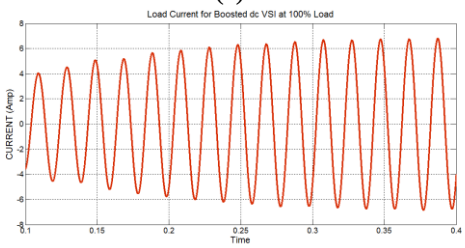
Here the time taken to attain steady state for these output quantities is found nearly to be 0.3 seconds due to boost circuit components (L1, C2, IGBT) in the boosted DC VSI.



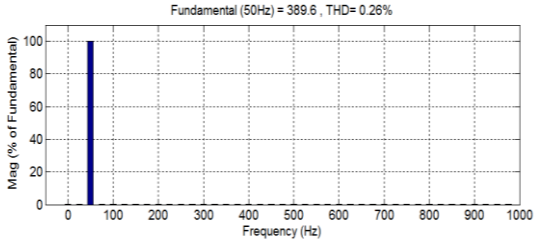
(a)



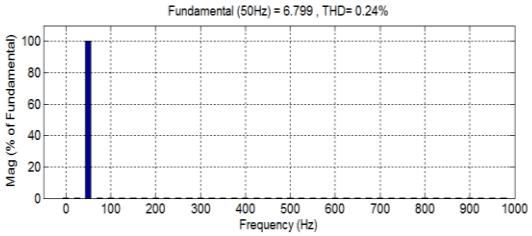
(b)

Figure 15 (a) voltage across (b) current through boosted DC VSI at full load

Fast fourier transform (FFT) analysis of output voltage and current at full load is shown in figure 16 for boosted DC VSI.



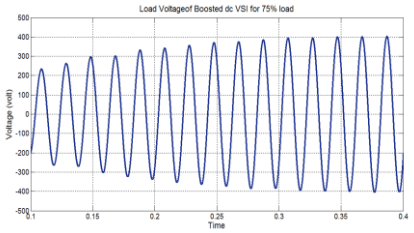
(a)



(b)

Figure 16 THD in (a) voltage (b) current for boosted DC VSI at full load

Figure 17 shows the output voltage across and current through load, when boosted DC VSI is loaded for 75% of the full load.



(a)

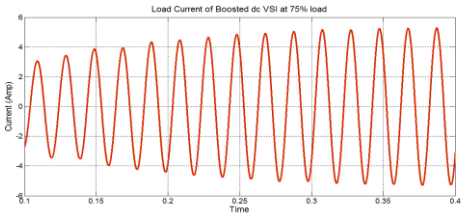
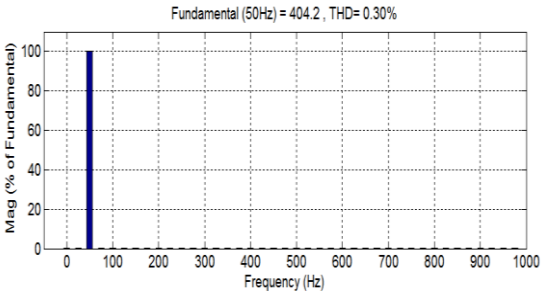
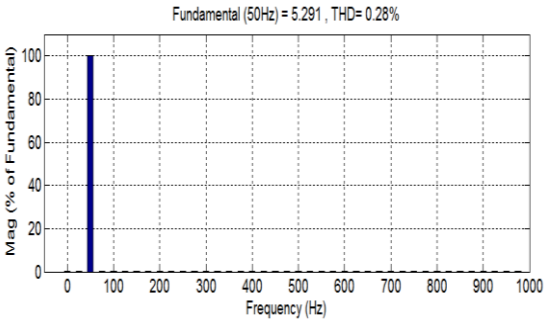


Figure 17 (a) voltage across (b) current through boosted DC VSI at 75%l load

Fast fourier transform (FFT) analysis of output voltage and current at load 75% of full load is shown in figure 18 for boosted DC VSI.



(a)



(b)

Figure18 THD in (a) voltage (b) current for boosted DC VSI at75% load

Figure 19 shows the output voltage across and current through load, when boosted DC VSI is loaded for 50% of the full load

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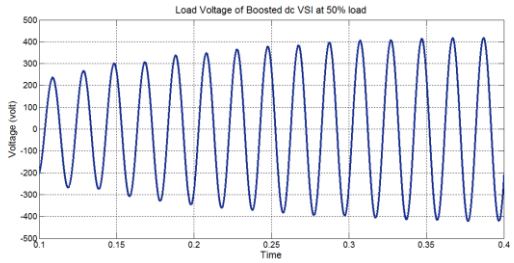
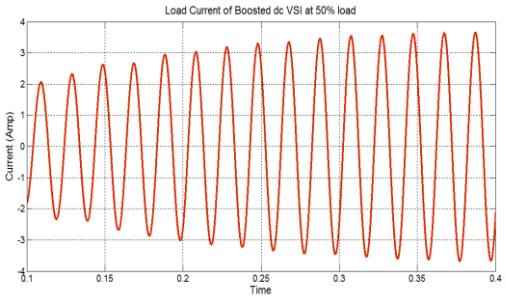


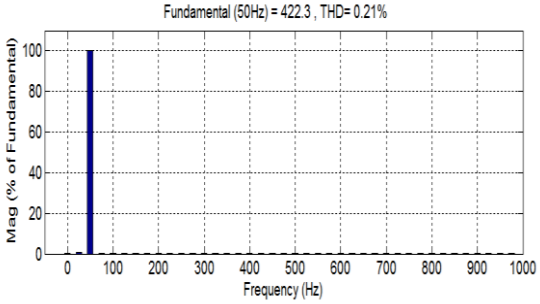
(a)



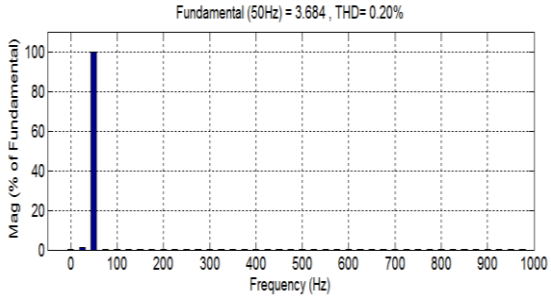
(b)

Figure 19 (a) voltage across (b) current through boosted DC VSI at 50% load

Fast fourier transform (FFT) analysis of output voltage and current at load 50% of full load is shown in figure 20 for boosted DC VSI.



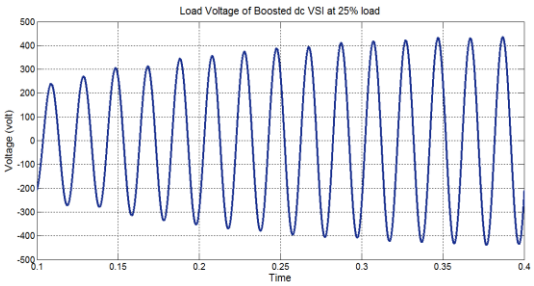
(a)



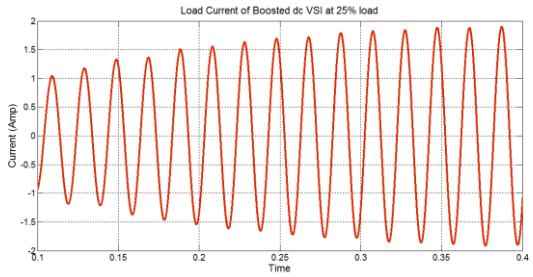
(b)

Figure 20 THD in (a) voltage (b) current for boosted DC VSI at 50% load

Figure 21 shows the output voltage across and current through load, when boosted DC VSI is loaded for 25% of the full load.



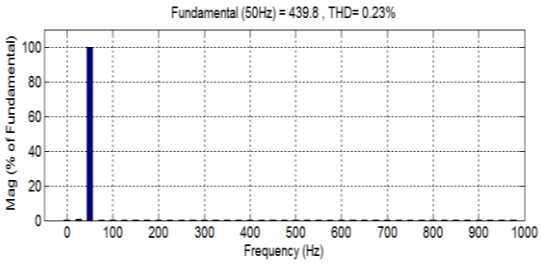
(a)



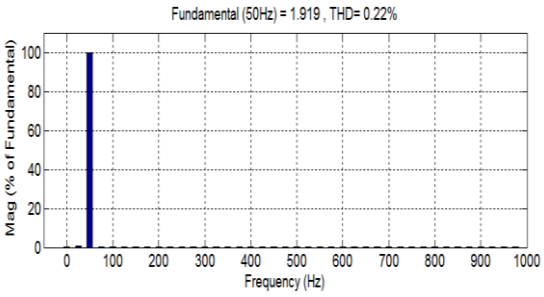
(b)

Figure 21 (a) voltage across (b) current through boosted DC VSI at 25% load

Fast fourier transform (FFT) analysis of output voltage and current at load 25% of full load is shown in figure 22 for boosted DC VSI



(a)



(b)

Figure 22 THD in (a) voltage (b) current for boosted DC VSI at 25% load

Figure 23 shows variation in voltage and current stresses on boost switch of boosted DC VSI with respect to load. The stresses are found to be decreasing with the increasing in the load.

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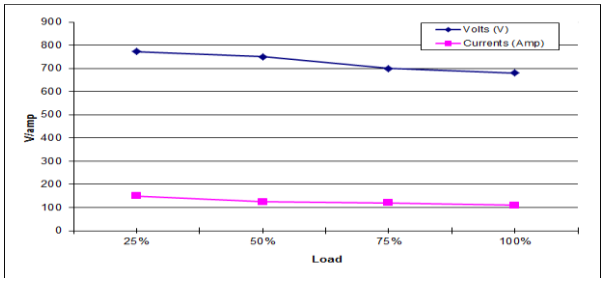

Figure 23 Variation in voltage and current stresses on boost switch of boosted DC VSI with respect to load

COMPARATIVE PERFORMANCE ANALYSIS OF BOOSTED DC VSI AND ZSI

Figure 24 shows the voltage stresses on switches of ZSI and boosted DC VSI. The stresses are found to less in case of ZSI for the same output conditions.

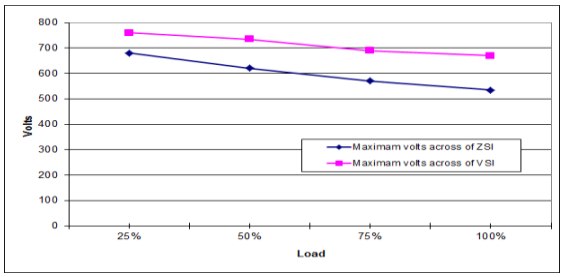

Figure 24 Voltage stresses on switches of ZSI and Boosted DC VSI

Figure 24 shows the current stresses on switches of ZSI and boosted DC VSI. The stresses are found to less in case of ZSI for the same output conditions.

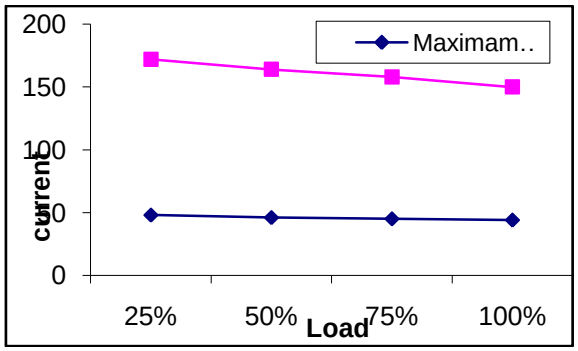

Figure 25 Current stresses on switches of ZSI and Boosted DC VSI

CONCLUSION

The Z-source inverter, when investigated, found to be satisfactory on the basis of boosting of voltage and quality of output voltage. Comparison with boosted DC VSI reveals if the stresses on the switches are properly managed, Z-source inverter, even in single-phase configuration gives better output.

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