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A Novel Logic Style used for Leakage Power Reduction in MOS Integrated Circuit

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Abstract: Full adders are necessary parts in applications corresponding to digital signal processors (DSP) architectures and microprocessors. Additionally to its main task, that is adding 2 numbers, it participates in several different helpful operations appreciate subtraction, multiplication, division, address calculation, etc. In most of those systems the adder lies in the critical path that determines the general speed of the system. Therefore enhancing the performance of the 1-bit full adder cell (the building block of the adder) could be a significant goal. Demands for the low power VLSI approaching the expansion of insistent design process to control use severely. To accomplish the rising demand, we advise a new low power adder by give up the MOS transistor calculate that reduce the grave threshold defeat so anew enhanced 14T CMOS l-bit full adder cell is specified in this paper. Results show five hundredth improvement in threshold loss drawback, 45% improvement in speed and considerable power consumption over the given adder and other different types of adders with comparable presentation.

Keywords: Arithmetic circuit, full adder, multiplier, low power, very Large-scale integration (VLSI).

I. INTRODUCTION

In practically all digital Integrated Circuit designs today, the addition procedure is one of the mainly necessary and frequent procedures. Instruction set for DSP's and all-purpose reason processors consist of at least one category of addition. Other commands like subtraction and multiplication make use of addition in their procedure and their underlying hardware is alike if not equal to addition hardware. Often, an Adder or multiple adders will be in the critical path of the preparation, hence the management of a recommend Will be often be limited by the performance of its adders.

When the designers look at further element of a chip, such as region or control, will find that the Hardware for addition will be a large contributor to these areas. It is then of assistance to choose the correct adder to implement in a design for the reason that the many feature it aspects in the overall chip. In this section we have reviewed several types of adders and studied their operation and performance. The various types of adders are

- Basic Adder Units
  - Half adder
  - Full adder
- Parallel Adders
  - Ripple carry adder
  - Carry look ahead adder.

A combinational circuit that adds two bits is known as a half adder. The half adder adds two single A and B Binary digits has two outputs, sum (S) and carry (C). With the combinational of an OR gate to join their carry outputs, two half adders be able to combined to create a full adder. Equations are the Boolean equations for sum and carryout.

$$Sum = a \oplus b \qquad (1)$$

$$Carry = a \cdot b \qquad (2)$$

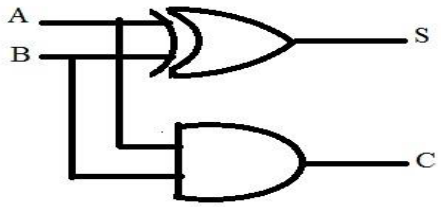

Fig. 1. Gate Schematic for Half Adder

A full adder joins three bits, the third bit produced from a preceding addition operation. A full adder combines binary figures and accounts for values carried in as well as out. A one-bit full adder join three one-bit numbers, frequently written as A, B, and Cin; operands are A and B, and Cin is a bit carried in from the next less considerable step.

$$S = A \oplus B \oplus C_{in} \qquad (3)$$

$$C_{out} = (A.\ B) + (C_{in}\ .\ (A \oplus B)) \qquad (4)$$

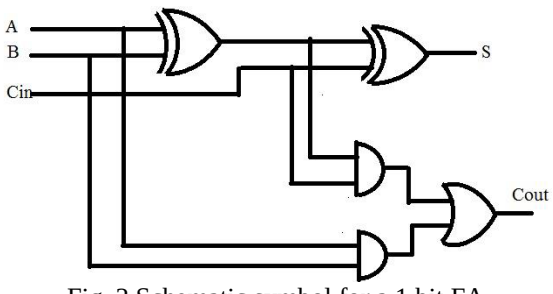

Fig. 2 Schematic symbol for a 1 bit FA

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II. METHOD

The Significant effort has been dedicated to explore new logic designs that transcend dynamic domino logic and CDL. Above all, source-coupled logic (SCL) has shown superior performance that's troublesome to realize exploitation the other logic vogue. However, it suffers from high power dissipation because of constant current draw and its differential nature needs complementary signals. Pseudo-nMOS logic, that uses one pMOS junction transistor as a pull-up device, provides high speed and low junction transistor count at the expense of high static power consumption moreover as reduced output voltage swing. Output prediction logic (OPL) has additionally shown superior performance in high speed adders. However, OPL needs the generation and distribution of multi-phase clock signals with little temporal arrangement separations and low skews that is troublesome to realize. whereas varied high speed logic designs are planned, dynamic and CDL still stay the foremost engaging selections once performance is that the primary concern.
Designers of digital circuits usually need quickest performance. This implies that the circuit desires high clock frequency. Because of the continual demand of increase operative frequency, energy economical logic vogue is usually vital in VLSI. Dynamic logic circuits are necessary because it provides higher speed and has lesser junction transistor demand in comparison to static CMOS logic circuits. CD logic provides an area window technique and a self-reset circuit that permits strong logical operation with decreased power consumption. The foremost distinct characteristic of CD logic from previously planned logic designs are that the delay. Unlike SCL, CD logic doesn't need complementary signals and might be simply integrated with static and dynamic domino logics. Also, CD logic doesn't have the matter of constant static power dissipation almost like pseudo-nMOS. Moreover, the clock temporal arrangement demand of CD logic isn't as demanding as OPL. CD logic can do strong operation with best performance as long as CLK signal arrives before the input signals. Constant delay (CD) logic vogue has been designed to mitigate the matter of high speed and noise margined.

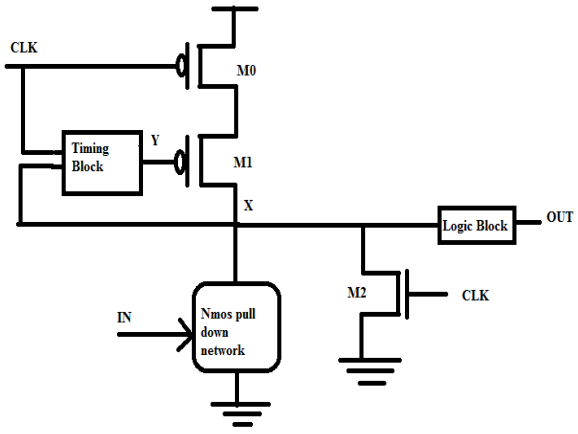

Fig. 3: Constant delay logic style

It outperforms different logic designs with higher energy potency. This high performance energy economical logic vogue has been wont to implement sophisticated logic expressions. It exhibits a novel characteristic wherever the output is pre-evaluated before the input from the preceding stage is prepared. Constant delay logic vogue that is employed for top speed applications is shown in Fig.3.

CD logic consists of 2 additional blocks. They're the timing block (TB) also because the logic blocks (LB). Temporal arrangement block consists of self reset technique and window adjustment technique. This allows strong logical operation with lower power consumption and better speed. Logic block reduces the unwanted defect and additionally makes cascading CD logic possible. The distinctive characteristic of this logic is that the output is pre- evaluated before the inputs from the preceding stage got prepared [3].

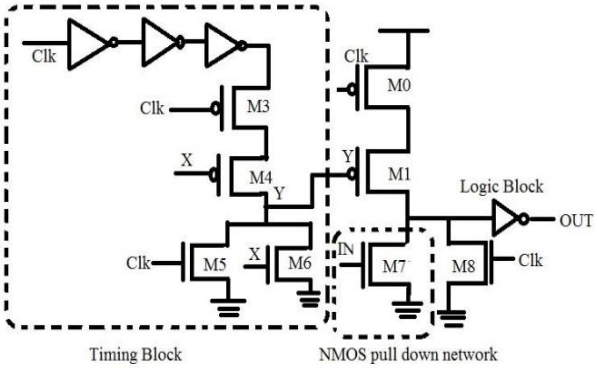

Fig. 4: Buffer diagram of CD logic style

The temporal order diagram for constant delay logic is shown in Fig. 5. CD logic works below 2 modes of operation.
i. Pre-discharge mode (CLK=1)
ii. Analysis mode (CLK=0)

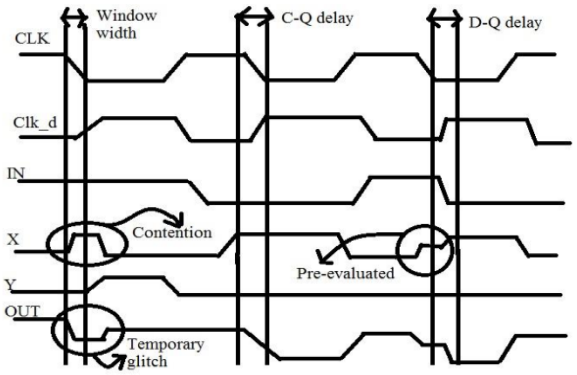

Fig. 5: Timing diagram of CD logic style

Pre-discharge mode happens once CLK is high and analysis mode happens once CLK is low. Throughout pre-discharge mode X and OUT are pre-discharged and pre-charged to GND and VDD severally. Throughout analysis mode 3 totally different conditions particularly contention, C-Q delay and D-Q delay takes place within the CD logic.

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Contention mode happens once IN=1 for the complete analysis amount. Throughout now a right away path current flows from pMOS to PDN. X raises to nonzero voltage level and OUT experiences a short lived bug. C-Q delay (clock-out) happens once IN goes to zero before CLK transits to low. At now X rises to logic one and OUT is discharged to VDD and also the delay is measured from CLK to Out. D-Q delay happens once IN goes to zero when CLK transits to low. Throughout now X initially enters contention mode and later rises to logic one and also the delay is measured from IN to Out.

III.RESULT

The maximum voltage is applying 5V to each circuit. The clock pulse is having the maximum amplitude of +5V to -5V.

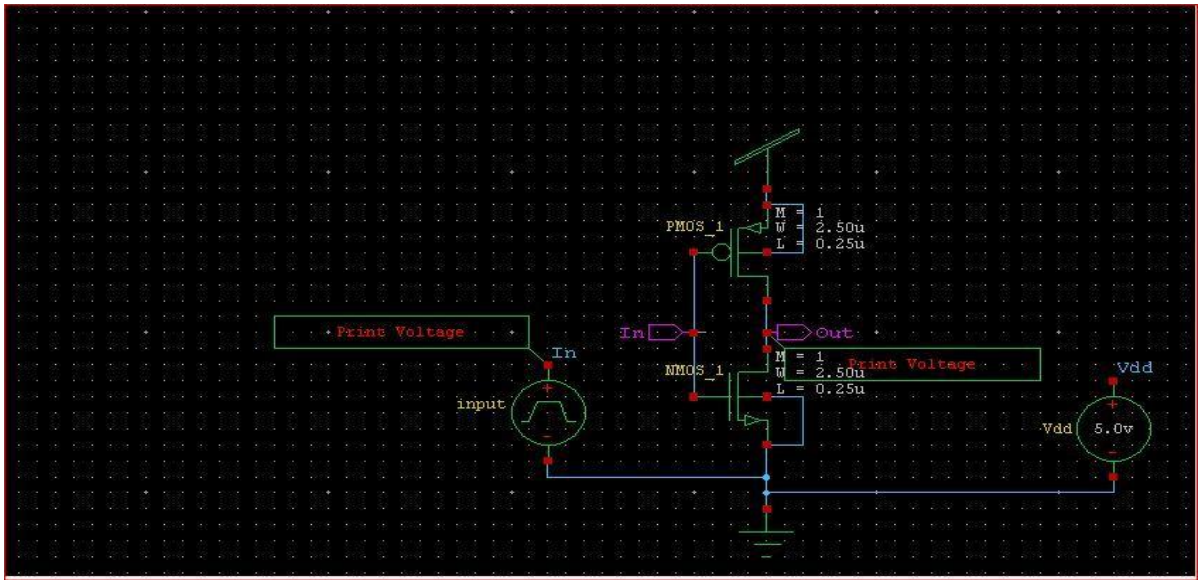

Fig. 6:- Schematic of Inverter

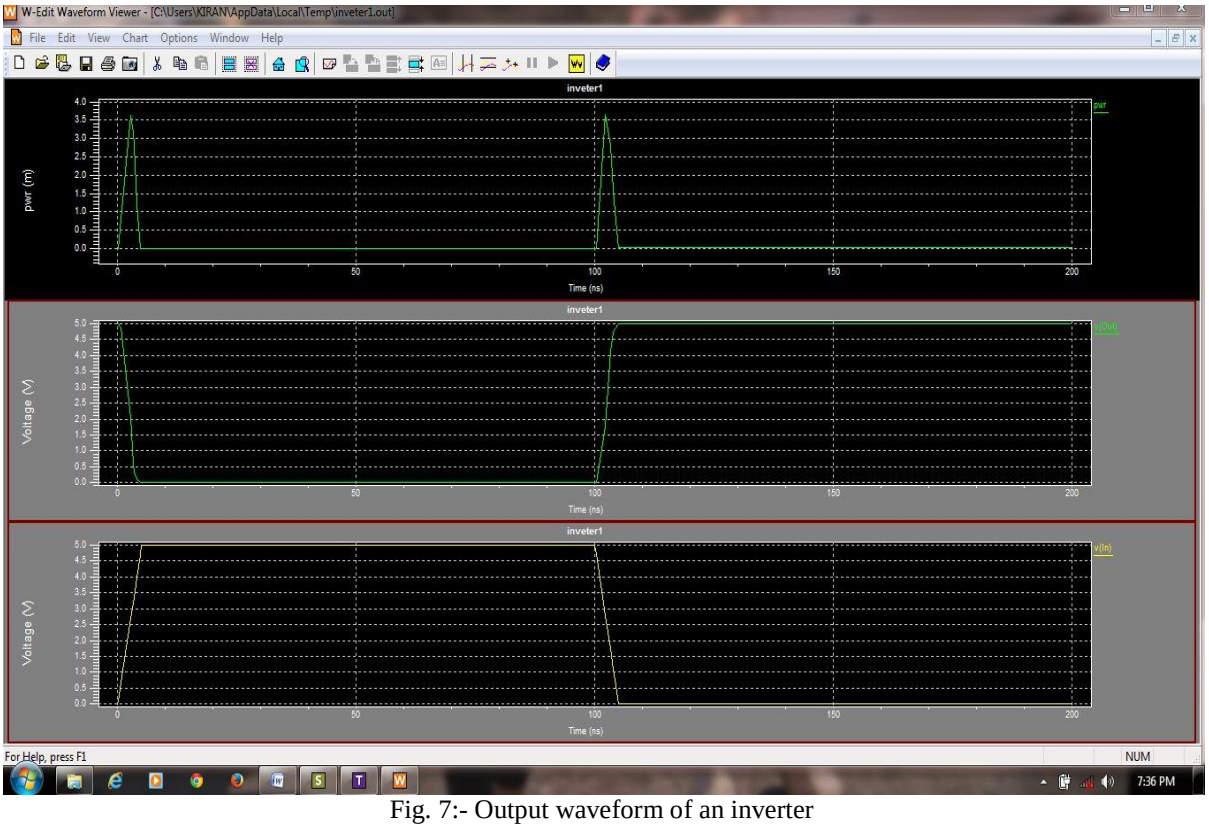

Fig. 7:- Output waveform of an inverter

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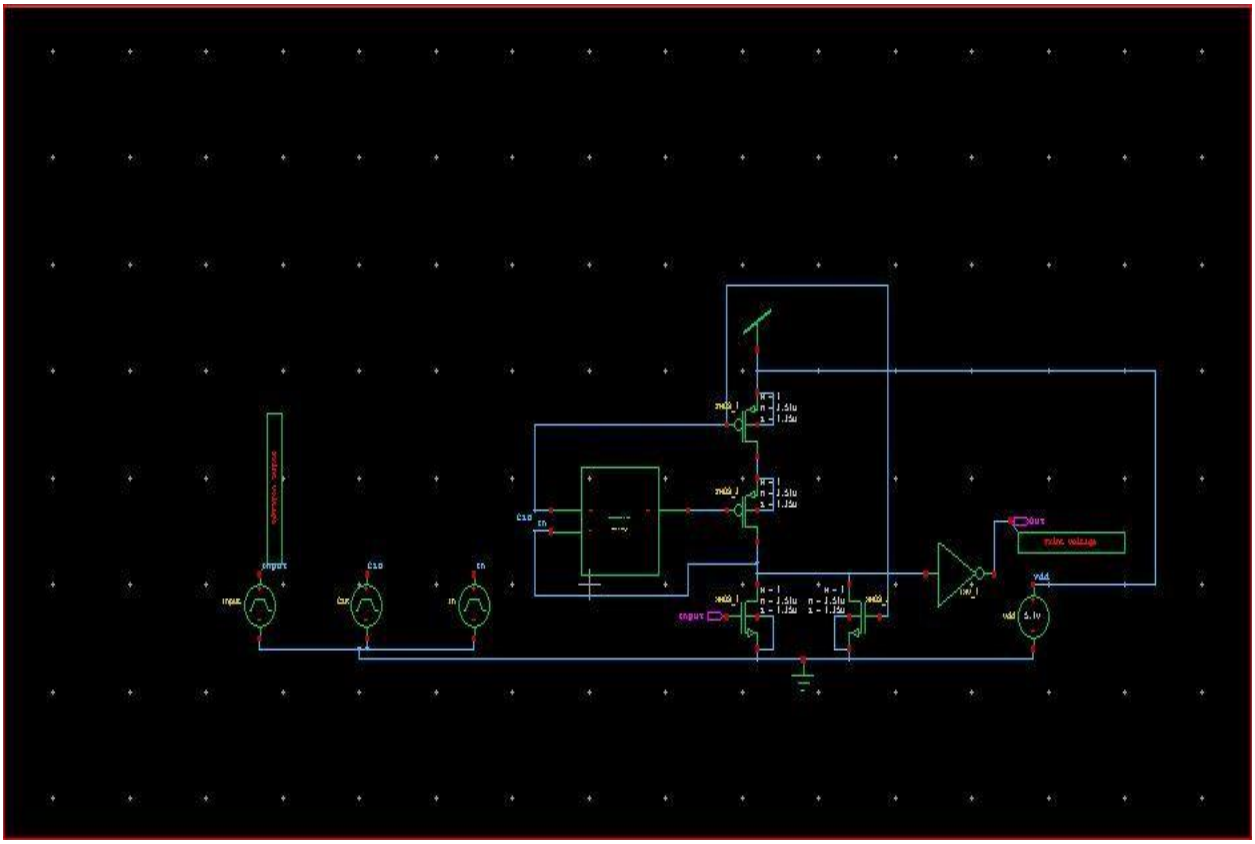

Fig. 8:- CD Inverter schematic

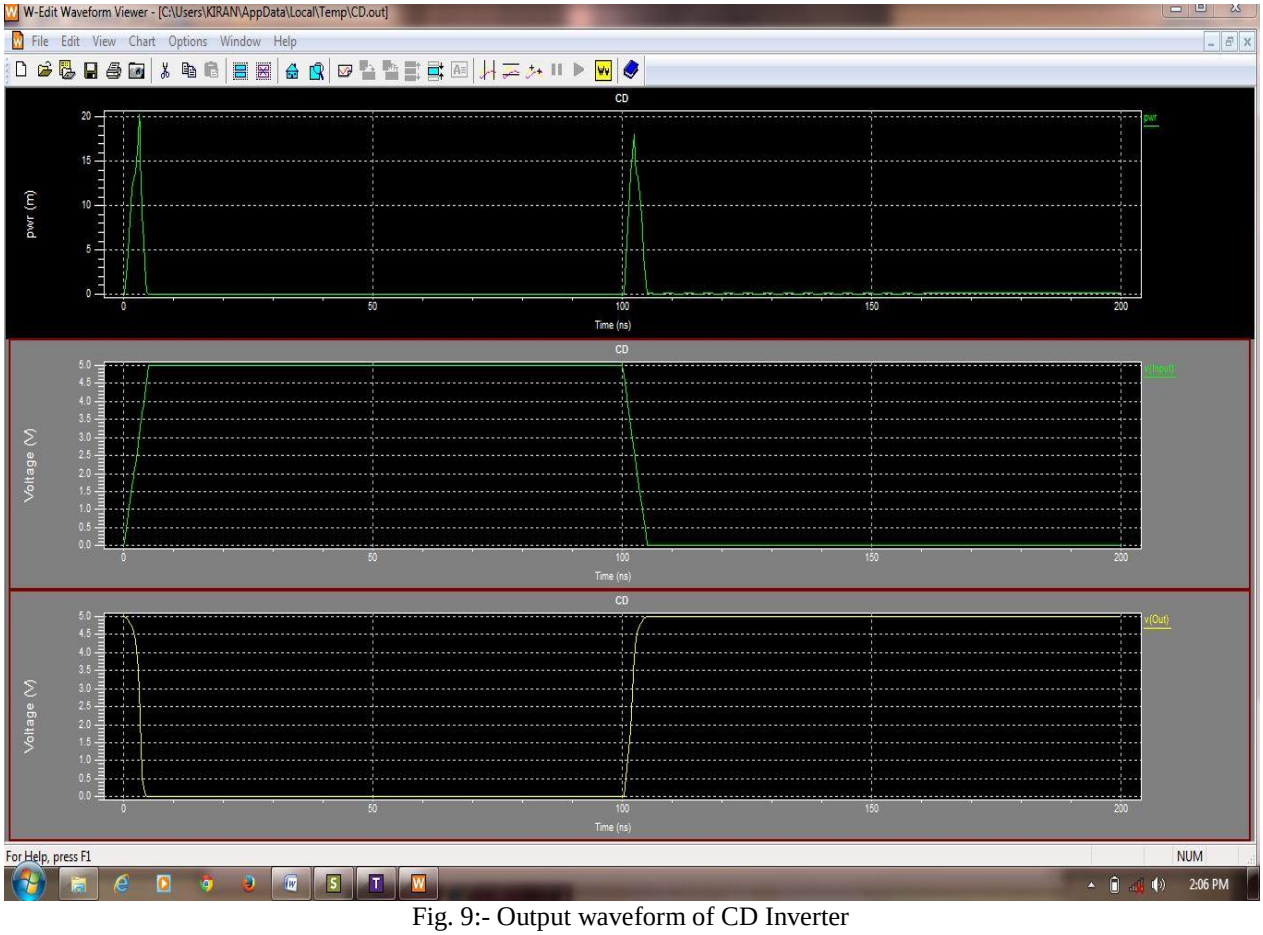

Fig. 9:- Output waveform of CD Inverter

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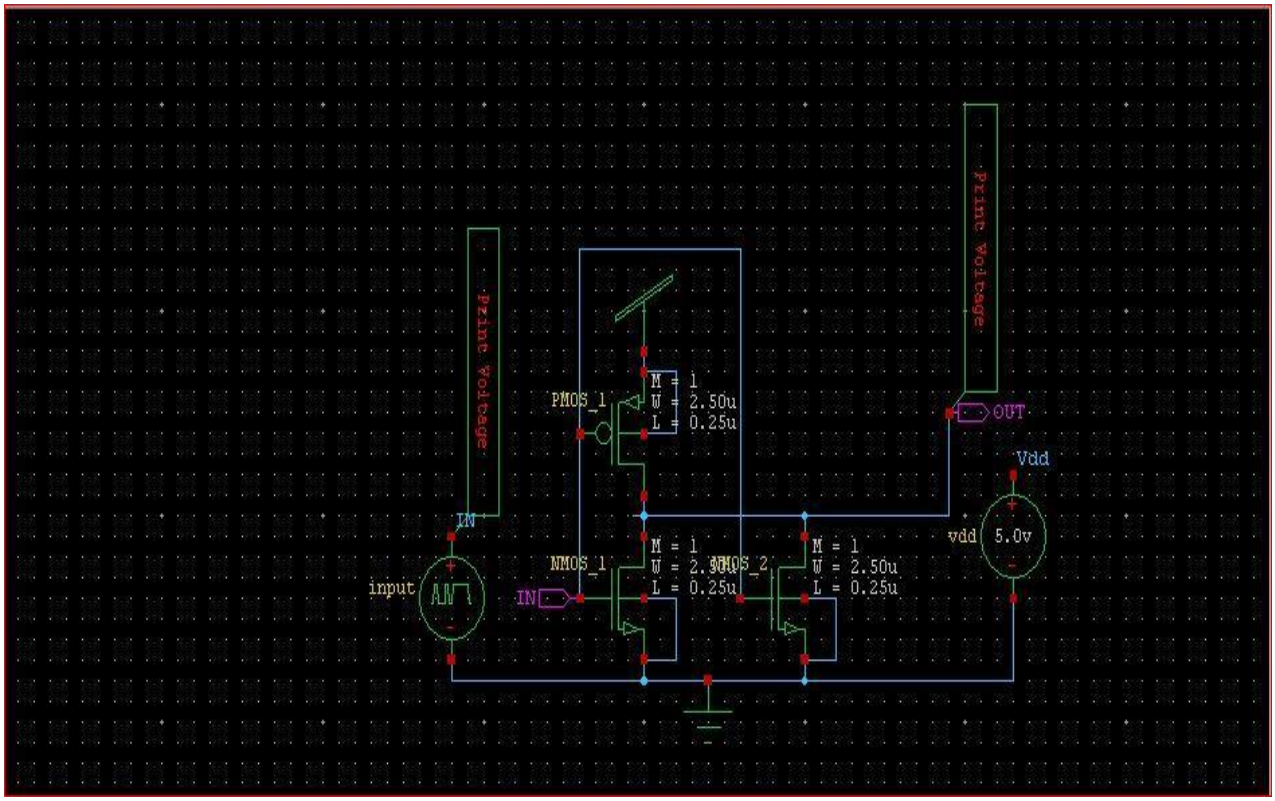

Fig. 10:- Clocked Inverter schematic

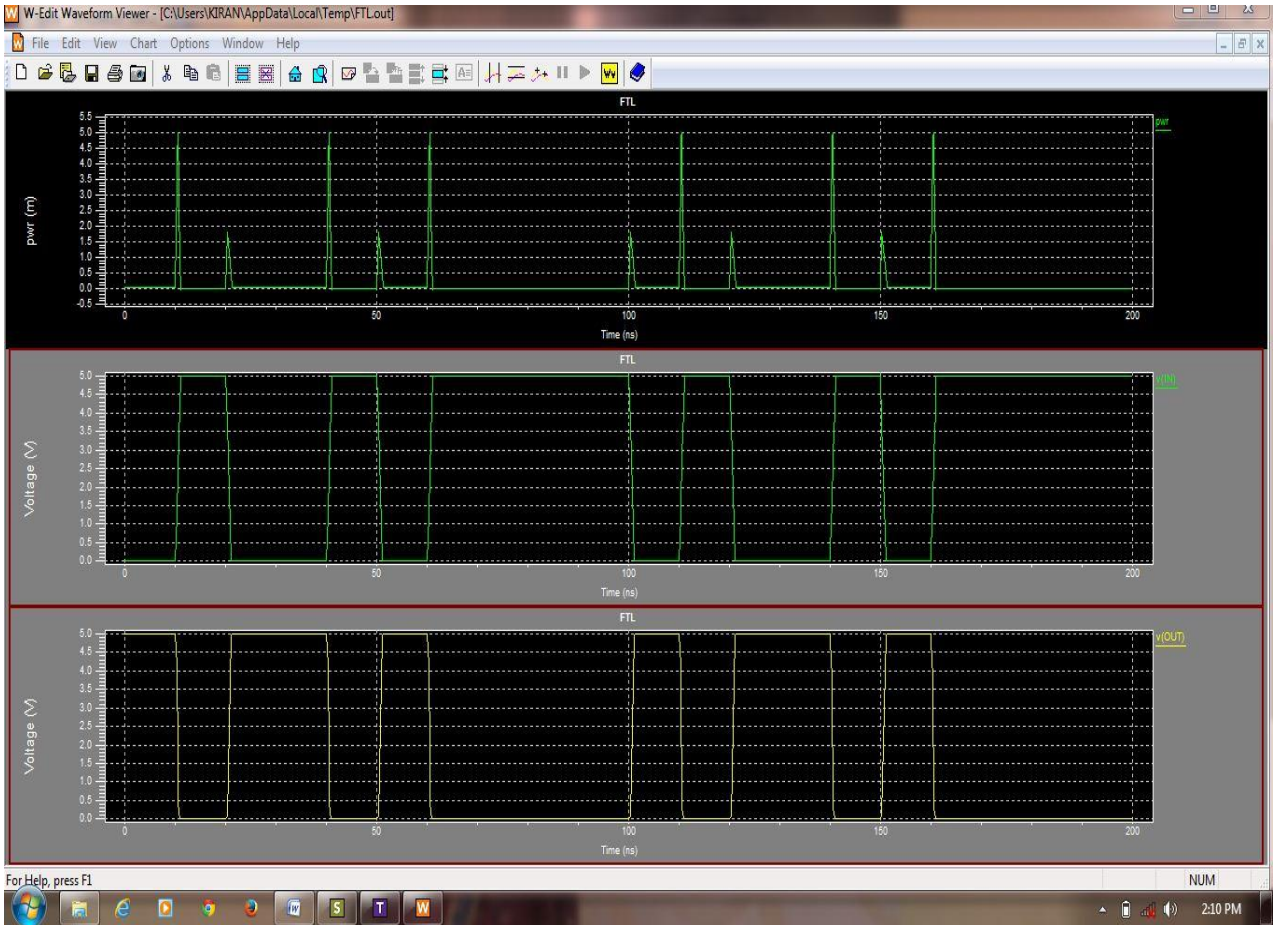

Fig. 11:- Output waveform of a Clocked Inverter

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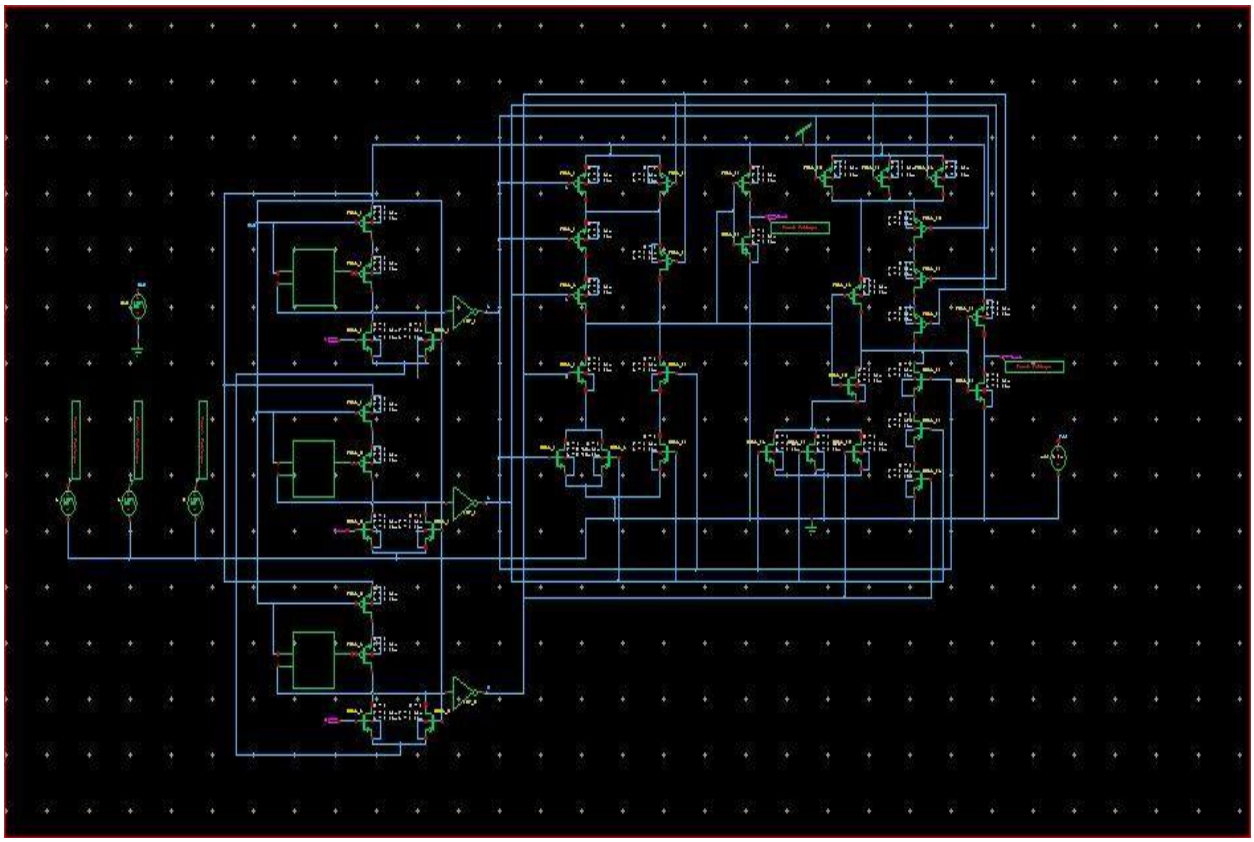

Fig.12:- CD Full Adder schematic

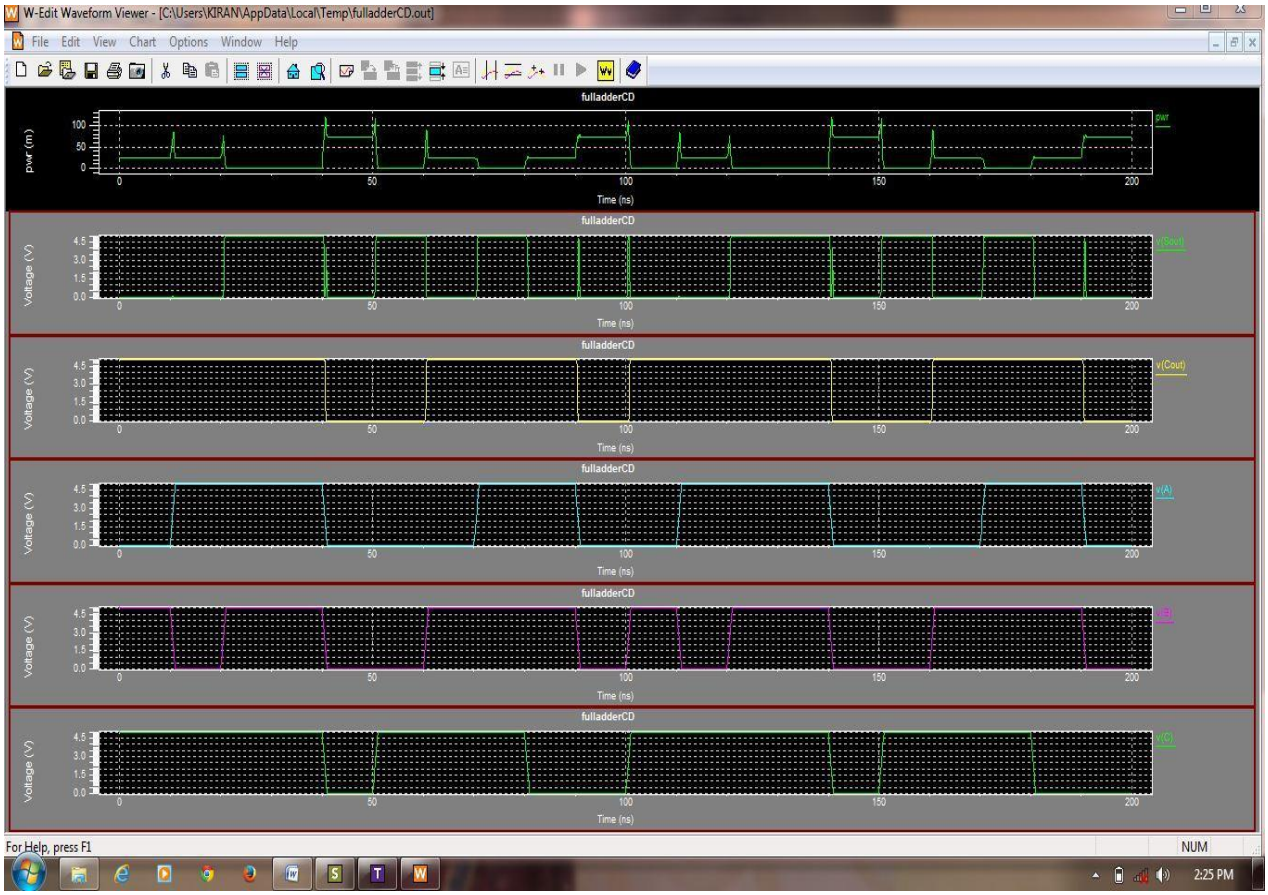

Fig. 13:- Output of a CD Full Adder

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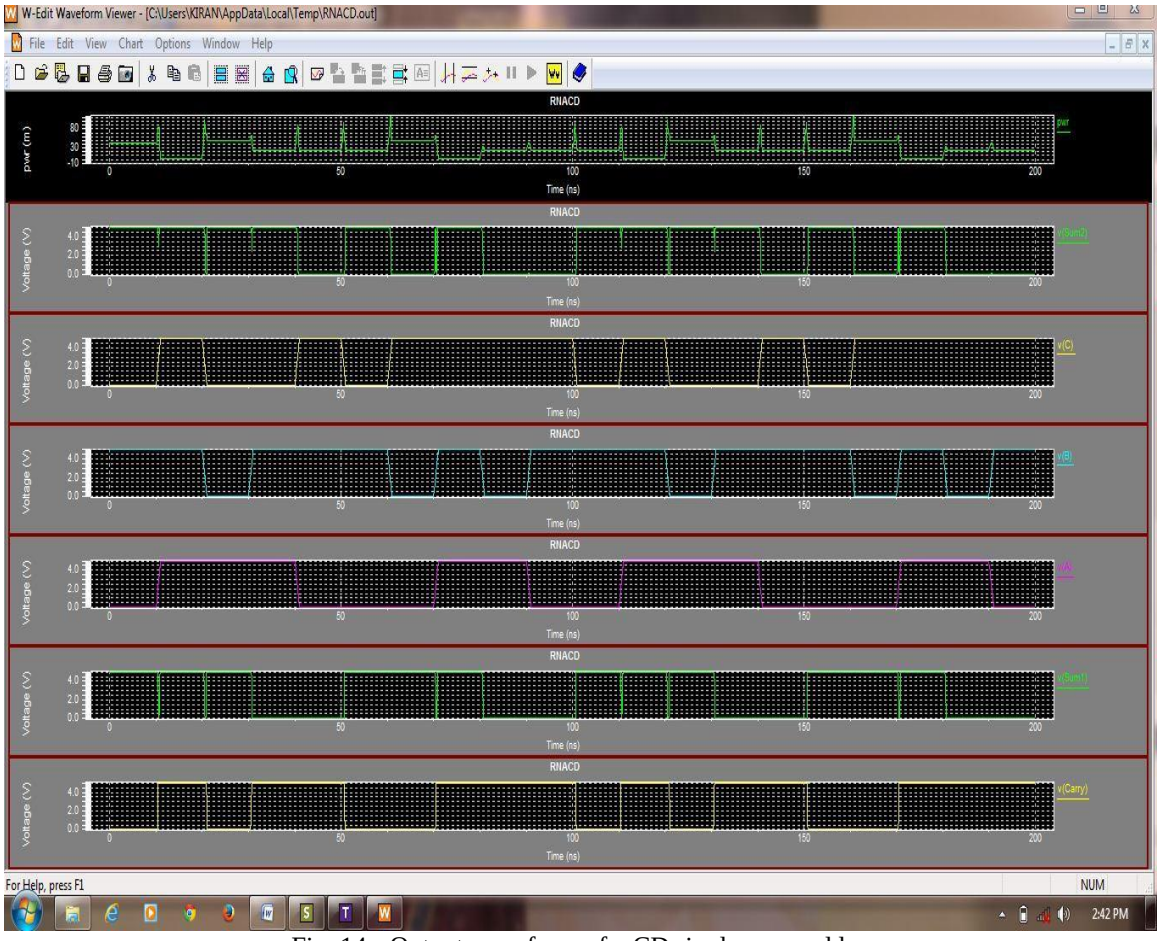

Fig. 14:- Output waveform of a CD ripple carry adder

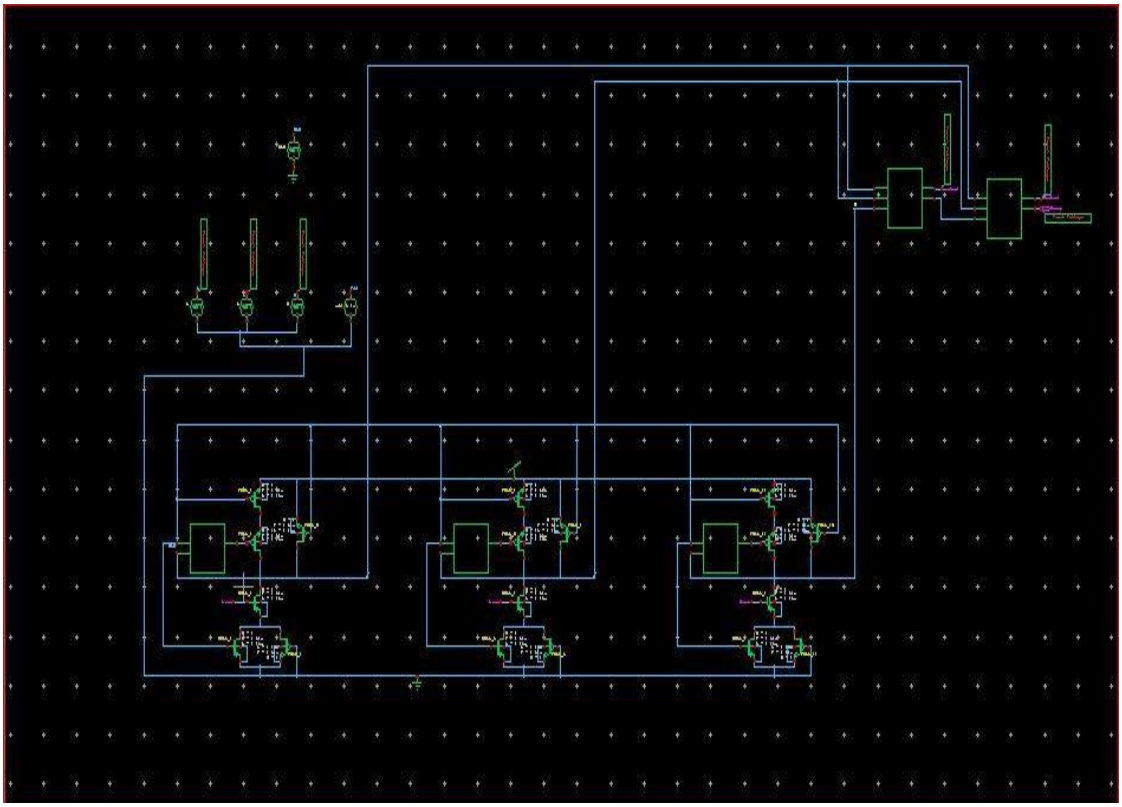
Fig. 15:- MCD Ripple Carry Adder schematic

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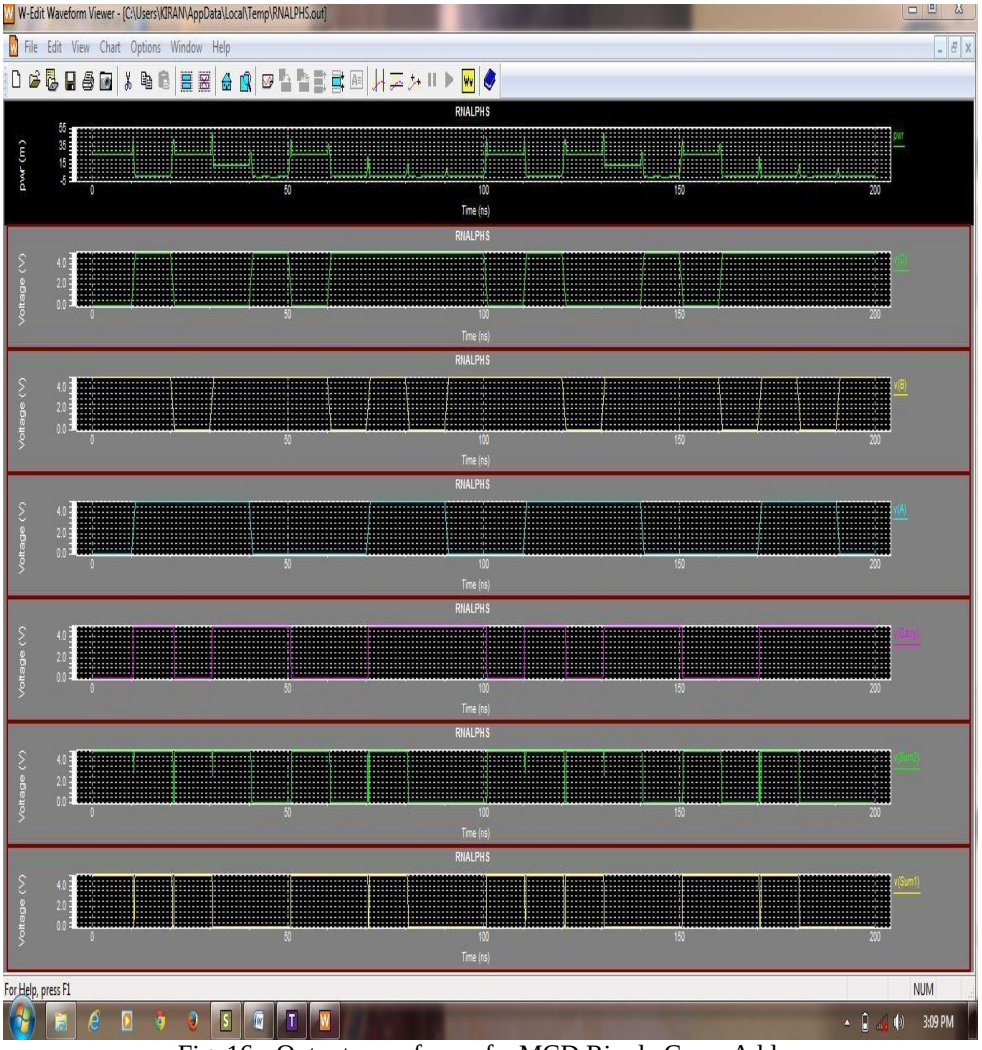

Fig. 16:- Output waveform of a MCD Ripple Carry Adder

IV. CONCLUSION

To overcome from the whole problem, changed constant delay logic vogue is planned. It will increase higher energy potency, performance and reduces the delay by exploitation the Tanner EDA software system. A brand new high performance changed constant delay logic vogue and Clocked logic vogue was planned. It will increase performance and reduces the facility as compared to the Constant delay logic vogue. Adders are designed exploitation each existing as well as planned logic. It is simulated in CMOS technologies for examination performance parameter power, rise-time and fall-time. From the result it's found that MCD and Clocked logic vogue has higher power than the present logic vogue.

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