ISSN 2393-8021

International Advanced Research Journal in Science, Engineering and Technology
Vol. 1, Issue 2, October 2014

Comparative Analysis of Power Factor Correction Techniques for AC/DC Converter at Various Loads

Nikita Kolte[1], N. B. Wagh[2]

M.Tech.Research Scholar, PEPS, SDCOE, Wardha(M.S.),India[1]

Associate Prof. Elect. Deptt.,DESCOET, Dhamangaon(M.S.),India[2]

Abstract: In this paper, two generalized topologies of single stage circuits such as Boost+flyback converter & Quasi active power factor correction (PFC) converter circuits are designed and their performance comparison is presented. Converters connected to the mains have the potential of injecting current harmonics that may cause voltage distortion. These harmonics can be significantly reduced if the input power factor is corrected by shaping the input current so that it is sinusoidal and in phase with the supply voltage. In the proposed quasi active PFC system, the power factor is drastically improved by using an auxiliary winding coupled to the transformer of a cascade dc/dc fly back converter. The proposed converter is presented and compared with boost+flyback converter for different loads and inputs. Simulations and analysis are carried out in MATLAB/SIMULINK with this control method for both systems and the results presented show the effectiveness of the improved converter topology.

Keywords: AC/DC converters, power factor correction (PFC), single stage, Fly back converter, total harmonic distortion (THD)

I. INTRODUCTION

Power supplies connected to ac mains introduce harmonic currents in the utility. It is very well known that these harmonic currents cause several problems such as voltage distortion, heating, noise and reduce the capability of the line to provide energy as per the standards and recommendations. This fact then forced to use power factor correction in power supplies.

Unity power factor and better output voltage regulation can be achieved with the very well known two stage approach, shown in Fig.1.Since the power stage is composed by two converters, size, cost and efficiency are penalized, mainly in low power applications. However, this is probably the best option for ac-dc converters due to the following reasons.

1) Sinusoidal line current guarantees the compliance of any Regulation.
2) It gives good performance under universal line voltage.
3) It offers many possibilities to implement both the isolation between line and load, and the hold-up time.
4) The penalty on the efficiency due to the double energy processing is partially compensated by the fact that the voltage on the storage capacitor is controlled. The fact of having a constant input voltage allows a good design of the second stage.

Although unity power factor is the ideal objective, it is not necessary for meeting the Regulations. For example, both IEEE 519 and IEC 1000-3-2, allow the presence of harmonics in the line current [1-2]. This fact has lead to propose solutions that obtain some advantages over the two stage approach.

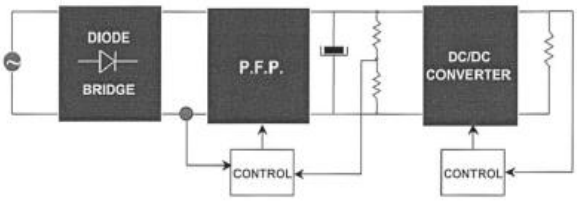

Fig.1 Two stage ac-dc PFC converter.

The main drawbacks of this scheme are its relatively higher cost and larger size resulted from its complicated power stage topology and control circuits, particularly in low power applications. In order to reduce the cost, the single-stage approach if hardware is implemented, this integrates the PFC stage with a dc/dc converter into one stage and has been elaborated and implemented [1-8]. These integrated single-stage power factor correction (PFC) converters usually use a boost converter to achieve PFC with discontinuous current mode (DCM) operation.

Some of these circuits are practical but others are too complex to be worth changing. The purpose of this project is to classify and compare several single stage converters proposed for the ac–dc conversion with power factor correction, having the two stage approach as a reference and focusing the study in the low power range.

In the proposed work, two generalized topologies of single stage circuits such as boost+flyback converter & quasi active power factor correction (PFC) converter circuits are designed and their performance comparison is presented.

ISSN 2393-8021

International Advanced Research Journal in Science, Engineering and Technology
Vol. 1, Issue 2, October 2014

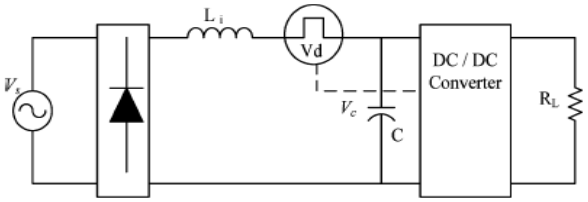

Fig 2 General circuit diagram of dither rectifier with single stage PFC cell.

In the proposed circuit, the power factor is improved by using an auxiliary winding coupled to the transformer of a cascade dc/dc fly back converter. The auxiliary winding is placed between the input rectifier and the low-frequency filter capacitor to serve as a magnetic switch to drive an input inductor. Since the dc/dc converter is operated at high-switching frequency, the auxiliary winding produces a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics are reduced. This technique eliminates the use of active switch and control circuit for PFC, which results in lower cost and higher efficiency. In order to achieve low harmonic content, the input inductor is designed to operate in discontinuous current mode.

II. PROPOSED QUASI ACTIVE PFC TECHNIQUE

In this work, a new technique of quasi-active PFC is proposed. The PFC cell is formed by connecting the energy buffer (L_B) and an auxiliary winding (L_A) coupled to the transformer of the dc/dc cell, between the input rectifier and the low-frequency filter capacitor used in conventional power converter. The input inductor operates in DCM such that a lower THD of the input current can be achieved [1].The proposed quasi-active PFC circuit is analyzed in this section. The circuit comprises a bridge rectifier, a boost inductor, a bulk capacitor Ca in series with the auxiliary winding, an intermediate dc-bus voltage capacitor, and a discontinuous input current power load, such as fly back converter. The fly back transformer (T) has three windings and the secondary winding $N_2 = 1$ is assumed. In the proposed PFC scheme, the dc/dc converter section offers a driving power with high- frequency pulsating source. The quasi active PFC cell can be considered as one power stage but without an active switch.

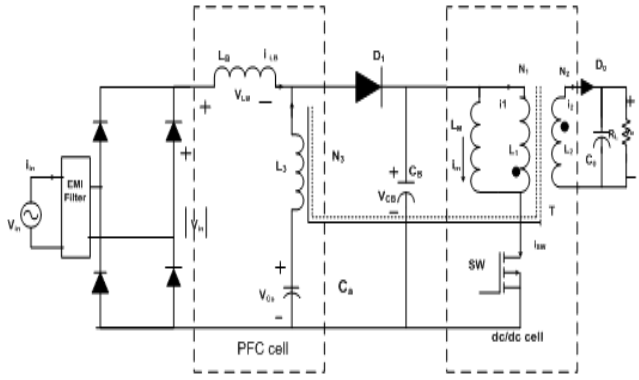

Fig 3 Proposed quasi-active PFC circuit

III. PRINCIPLE OF OPERATION OF THE PROPOSED QUASI ACTIVE PFC CIRCUIT

To simplify the analysis, following assumptions have been made.

1) All semiconductors components are ideal. According to this assumption, the primary switch and the rectifiers do not have parasitic capacitances and represent ideal short and open circuits in their ON and OFF states, respectively.

2) The power transformer does not have the leakage inductances because of the ideal coupling.

3) All the capacitors are high enough so that the voltage across them is considered constant.

4) Finally, the input voltage of the converter is considered constant during a switching cycle because the switching frequency is much higher than the line frequency.

To facilitate the analysis of operation, Fig. 4(a) and (b) shows the topological stages and the key waveforms of the proposed circuit. It is assumed that both the input inductor L_B and the magnetizing inductance of the flyback converter operate in DCM. Therefore, currents i_{LB} , i_m, and i_2 are zero at the beginning of each switching period. It is also assumed that the average capacitor voltage V_{Ca} is greater than the average rectified input voltage $|v_{in}|$.

To ensure proper operation of the converter, the transformer's turns ratio should be $(N_1/N_3) \geq 2$ and the boost inductor $L_B < L_m$. In steady-state operation, the topology can be divided into four operating stages.

1) Stage 1 ($t_o - t_1$):

When the switch (SW) is turned on at $t = t_o$, diodes D_1 and D_o are OFF, therefore, the dc-bus voltage V_{CB} is applied to the magnetizing inductor L_m, which causes the magnetizing current to linearly increases. This current can be expressed as

$$i_m = \frac{V_{CB}}{L_m}(t_0 - t_1) \qquad (1)$$

And since diode D_1 is OFF, the input inductor L_B is charged by input voltage, therefore, the inductor current i_{LB} is linearly increased from zero since it is assumed that the PFC cell operates in DCM.

This current can be expressed as

$$i_{LB} = \frac{|V_{in}| + \left(\frac{N_3}{N_1}\right)V_{CB} - V_{Ca}}{L_B}(t_0 - t_1) \qquad (2)$$

Where, $V_{in} = V_m|\sin\theta|$ is the rectified input voltage, $(t_o - t_1) = dT_S$ is the ON-time of the switch (SW), L_B is the boost inductor and N_1, N_3 are the primary and auxiliary turns ratio, respectively. At this stage, $i_{LB} = -i_3$ and the capacitor C_a is in the charging mode. On the other hand, D_o is reversed biased and there is no current flow through the secondary winding. Since the transformer is assumed ideal, based on Ampere's law, it has

$$N_1 i_1 + N_2 i_2 - N_3 i_{LB} = 0$$

Where $i_2 = 0$ at this stage therefore,

$$i_1 = \frac{N_3}{N_1} i_{LB} = -\frac{N_3}{N_1} i_3 \qquad (3)$$

ISSN 2393-8021

International Advanced Research Journal in Science, Engineering and Technology
Vol. 1, Issue 2, October 2014

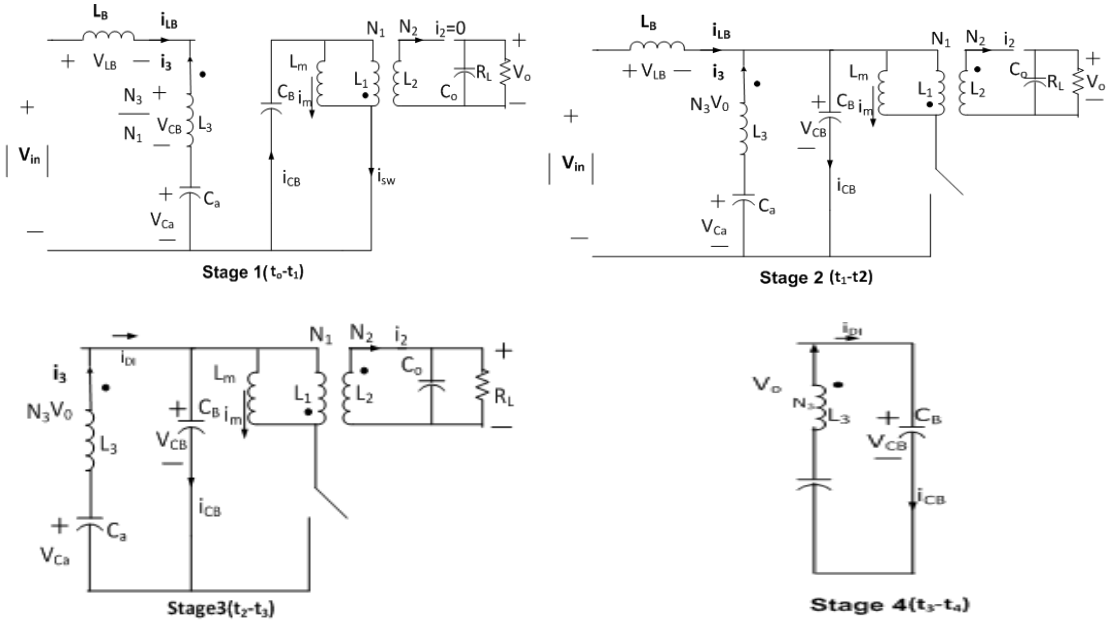

Fig. 4(a) Equivalent circuit operation stages of the proposed PFC circuit during one switching period

Thus

$$i_m = i_{CB} - i_1 = i_{CB} + \frac{N_3}{N_1} i_3 \qquad (4)$$

Therefore, from (4) it can be seen that the magnetizing current i_m is supplied by the discharging current from the dc bus capacitor C_B and the current i_3 which is equal to input current i_{LB} at this stage. The current through the main switch (SW) is given by

$$i_{SW} = i_{CB} = i_m - \frac{N_3}{N_1} i_3 = i_m + \frac{N_3}{N_1} i_{LB} \qquad (5)$$

Therefore, the current stress of the switch can be reduced by selecting the turn's ratio (N_3/N_1), which is designed to be less than 1 to ensure proper operation of the transformer. Compared to the single-stage BIFRED converter, the switch current is given by

$$i_{SW} = i_m + i_{LB} \qquad (6)$$

Obviously, the proposed circuit has less switch current stress, therefore, the conduction loss and switching losses are reduced, and the efficiency is improved correspondingly. This stage ends when the switch is turned off at $t = t_1$.

2) Stage 2 ($t_1 - t_2$): When the switch is turned OFF at $t = t_1$, output diode D_o begins to be forward biased. Therefore, the energy stored in the transformer magnetizing inductor is delivered to the load through the secondary winding. Similarly, the diode D_1 is also forward biased and the voltage across L_B now $V_{in} - V_{CB}$. Therefore, the current I_{LB} is linearly decreased to zero at $t = t_2$ (DCM operation), and the energy stored in L_B is delivered to the dc bus capacitor C_B. Therefore

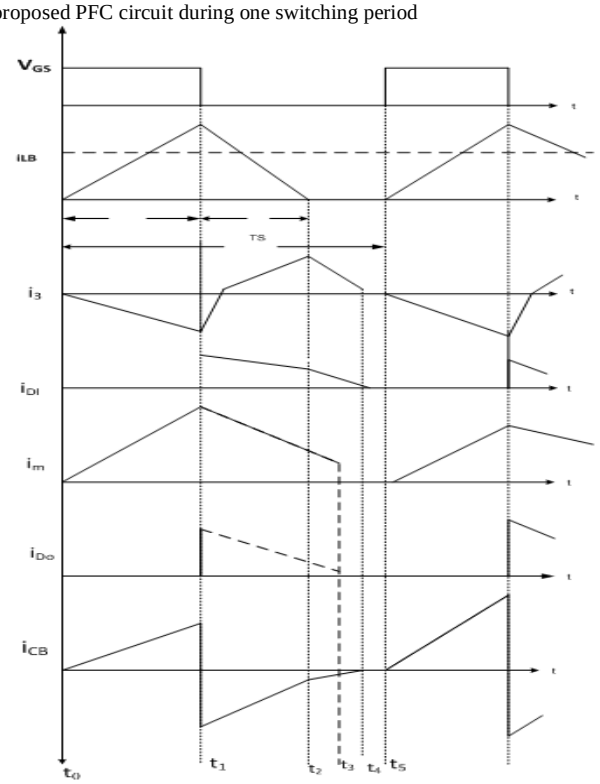

Fig. 4 (b) Key switching waveforms of the proposed PFC technique

$$i_{LB} = \frac{|V_{in}| - V_{CB}}{L_B}(t_1 - t_2) \qquad (7)$$

The capacitor (Ca) is also discharging its energy to the dc bus capacitor C_B and the current i_3 reverse its direction. Therefore, the capacitor current is given by

$$i_{D1} = i_{CB} = i_{LB} + i_3 \qquad (8)$$

3) Stage 3 ($t_2 - t_3$): At this stage, the input inductor current i_{LB} reaches zero and the capacitor Ca continues to discharge its energy to the dc bus capacitor C_B. Therefore, $i_{D1} = i_{CB} = i_3$. At $t = t_3$, the magnetizing inductor releases

ISSN 2393-8021

International Advanced Research Journal in Science, Engineering and Technology
Vol. 1, Issue 2, October 2014

all its energy to the load and the currents i_m and i_2 reach to zero level because a DCM operation is assumed.

4) Stage 4 ($t_3 - t_4$): This stage starts when the currents i_m and i_2 reach to zero. Diode D_1 still forward biased, therefore, the capacitor Ca still releasing its energy to the dc bus capacitor C_B. This stage ends when the capacitor Ca is completely discharged and current i_3 reaches zero. At $t = t_5$, the switch is turned on again to repeat the switching cycle.

IV. STEADY STATE ANALYSIS OF QUASI ACTIVE PFC CIRCUIT

The steady state analysis of quasi active converter has been explained with mathematical analysis .The voltage conversion ratio of the proposed converter can be estimated from the volt-second balance on the inductors and the input–output power balance as explained in the following. From the volt-second balance on L_B

$$\left(\mathrm{Vin} + \left(\frac{\mathrm{N3}}{\mathrm{N1}}\right)\mathrm{VCB} - \mathrm{Vca}\right)\mathrm{dTs} = (\mathrm{VCB} - \mathrm{Vin})\mathrm{d1Ts} \quad (9)$$

Where d_1 is the OFF-time of the switch (SW). Therefore, d_1 could be given by

$$\mathrm{d1} = \frac{\mathrm{Vin} + (\mathrm{N3}/\mathrm{N1})\mathrm{VCB} - \mathrm{Vca}}{\mathrm{VCB} - \mathrm{Vin}}\,\mathrm{d} \quad (10)$$

From Fig.4 (b), the average current of the boost inductor in a switching cycle is given by

$$\mathrm{Iin} = \mathrm{i_{LB,av}} = \frac{\mathrm{i_{LB,peak}}}{2}(\mathrm{d} + \mathrm{d1})\mathrm{Ts} \quad (11)$$

Substituting for $i_{LB,\,peak}$ given in (2) and using (10), the average input current is given by

$$\mathrm{Iin} = \frac{\mathrm{Vin} + (\mathrm{N3}/\mathrm{N1})\mathrm{VCB} - \mathrm{Vca}}{2\mathrm{L_B}}\mathrm{d^2Ts} \times \left(\frac{(1 + \mathrm{N3}/\mathrm{N1})\mathrm{VCB} - \mathrm{Vca}}{\mathrm{VCB} - \mathrm{Vin}}\right) \quad (12)$$

It can be seen that to reduce the dead time and improve the power factor of the input current the turn's ratio must be ≥0.5. However, higher V_{CB} means higher voltage stress on the power switch (SW), which can reduce the efficiency of the converter. Therefore, a tradeoff between THD and efficiency must be made. The energy absorbed by the circuit from the source during a half switching cycle is given by

$$\mathrm{P_{in}} = \frac{1}{\pi}\int_0^{\pi} Vm\sin(t)\,Iin\,dt$$

Substitution for I_{in} in given (12) yields

$$\mathrm{P_{in}} = \frac{1}{\pi}\frac{Vm}{2L_B}d^2Ts(A)\int_0^{\pi}\sin(t)\,B\,dt \quad (13)$$

Where

$$A = (1 + N3/)VCB - Vca$$

$$B = \frac{Vm\,sin\,(t) + (N3/N1)VCB - Vca}{VCB - Vm\,sin\,(t)}$$

The average output power for a DCM flyback converter is given by

$$\mathrm{Po} = \frac{VCB^2}{2Lm}\,d^2\,Ts \quad (14)$$

Assume 100% efficiency, $P_{in} = P_o$, yields

$$VCB^2 = \frac{Vm}{\pi}\frac{Lm}{L_B}(A)\int_0^{\pi} sin(t)\,B\,dt \quad (15)$$

Equation (15) shows that the dc bus capacitor is independent of load variation; V_{CB} is determined by the input voltage and circuit parameters L_m/L_B, N_3/N_1.

V. SYSTEM SIMULATION & OUTPUTS

A. MATLAB Simulation Model of Boost+flyback Converter With R Load **:-**

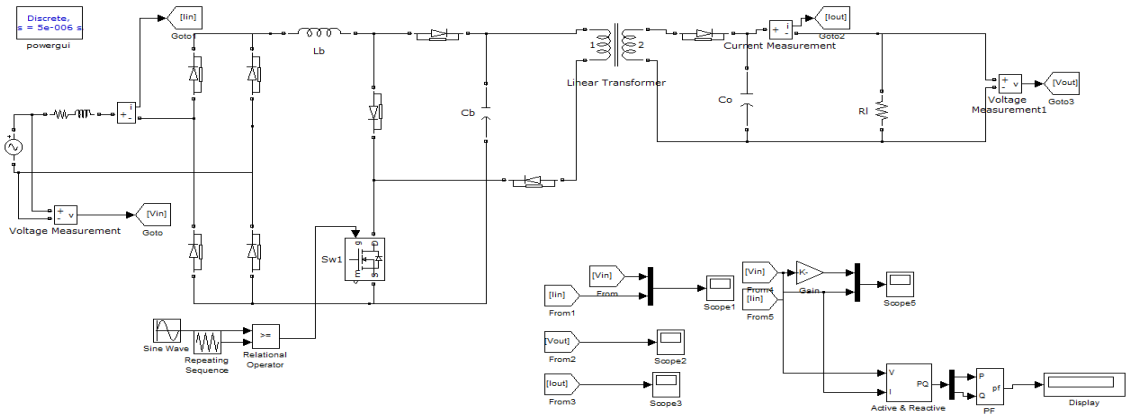

Fig.5 System Model of Boost+flyback converter (R Load) in MATLAB

ISSN 2393-8021

International Advanced Research Journal in Science, Engineering and Technology
Vol. 1, Issue 2, October 2014

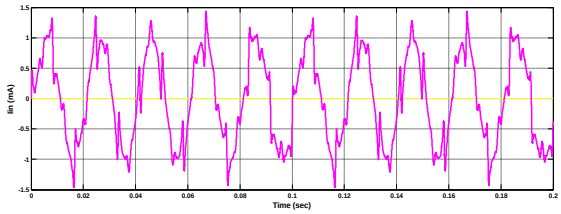

Fig.6 (a) Input current waveform (R Load)

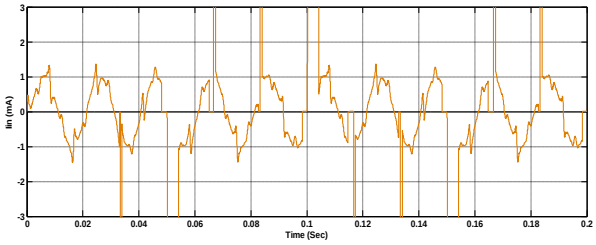

Fig. 6(b) Input current waveform (RL Load)

B. MATLAB Simulation Model Of Quasi Active PFC Converter with R Load:-

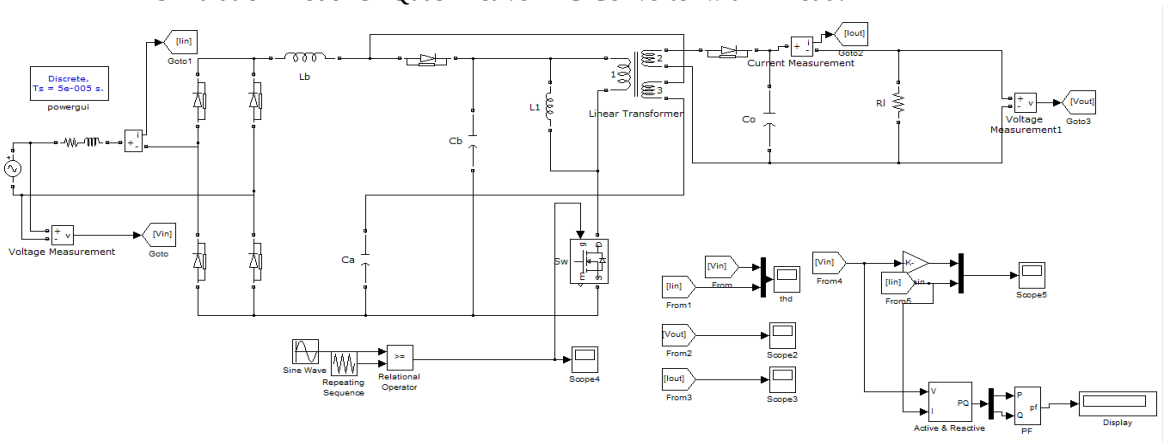

Fig.7 System Model of Proposed converter (R Load) in MATLAB

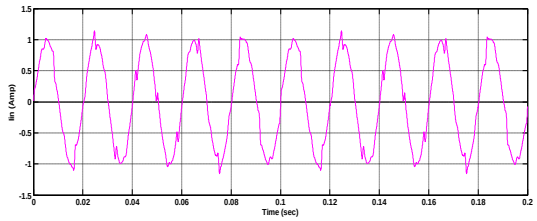

Fig. 8(a) Input current waveform (R Load)

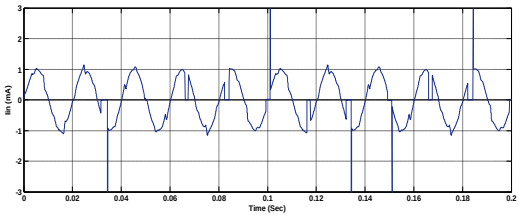

Fig.8 (b) Input current waveform (RL Load)

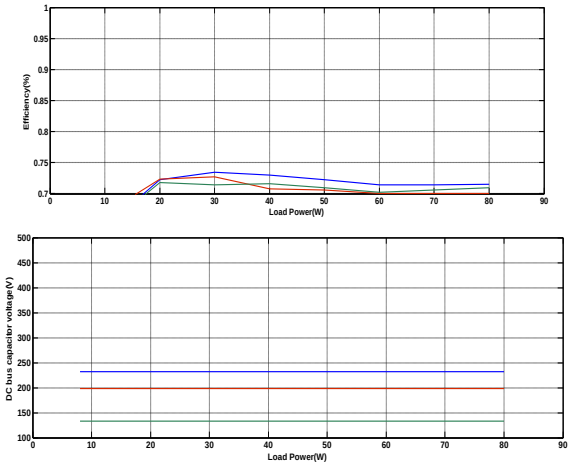

Fig.9 Measured efficiency versus load power for a range of input voltage

ISSN 2393-8021

International Advanced Research Journal in Science, Engineering and Technology
Vol. 1, Issue 2, October 2014

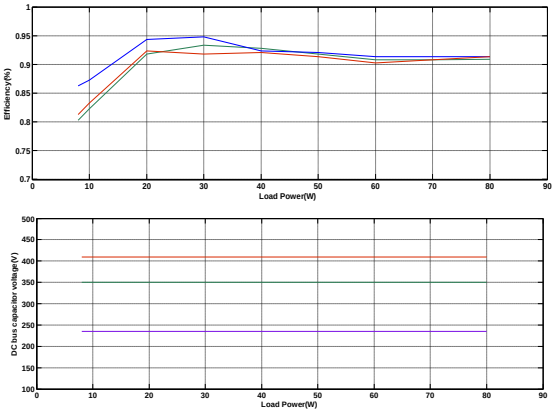

Fig.10 Measured efficiency versus load power for a range of input voltage

VI. RESULTS & DISCUSSION

Table 1. Input power factor at different loads and input voltages

	Boost+flyback converter			Proposed converter		
	V_{in}= 100 V					
	No Load	R Load	RL Load	No Load	R Load	RL Load
Input Power Factor	0.7677	0.9572	0.8306	0.8749	0.9984	0.9983
	V_{in}= 180 V					
	0.7669	0.8136	0.8275	0.8739	0.9984	0.9996
	V_{in}= 220 V					
	0.7667	0.8136	0.8268	0.8736	0.9984	0.9999

In this the two PFC schemes i.e. boost+flyback converter & proposed Quasi active converter are designed by using MATLAB and various simulation results are obtained. Fig.6 (a) and fig.6 (b) shows the input current waveforms of boost+flyback converter and fig.8 (a) and fig.8 (b) shows the input current waveforms of proposed Quasi active converter for R and RL load respectively. It has been observed that the input current waveform is more distorted for RL load as compared to R load. Current waveform shows a value of 1.125 mA for R load when V_{in} =100 V is applied. The power factor of rectifier obtained for R load with boost+flyback converter & quasi active converter is 0.9572 & 0.9984 respectively and that for RL load is 0.8306 & 0.9983 respectively. Hence for purely resistive load, it gives improved power factor than inductive load.

Power factor is observed for different loads & various inputs as shown in table 1. After comparing both PFC techniques i.e. boost+flyback converter & proposed Quasi active converter, it is seen that proposed converter gives improved power factor for different loads & various inputs. The THD measured for boost+flyback converter is 28.55% and that for quasi active converter is 4.19%. After comparing it is observed that boost+flyback converter gives 70-75% efficiency for different input voltages. Whereas quasi active converter gives efficiency above 90% hence quasi active PFC technique is more efficient method than boost+flyback technique.

VII. CONCLUSION

From the simulation results, it is concluded that the proposed quasi active PFC method produces a current with low harmonic content to meet the standard specifications as well as high efficiency as compared to conventional boost+flyback converter. This circuit is based on adding an auxiliary winding to the transformer of a cascade dc/dc DCM fly back converter. The input inductor can operate in DCM to achieve lower THD and high power factor. The DCM fly back converter was designed and implemented for 50 V/80 W output. The measured THD = 4.19% and the power factor of unity is obtained for RL Load. The proposed converter can maintain 90% efficiency or above at high load but boost+flyback converter gives 70-75% efficiency at high loads. Thus the proposed quasi active PFC technique is the efficient system for improving power factor of rectifiers.

REFERENCES

[1] Hussain S. Athab, and Dylan Dah-Chuan Lu, "A High-Efficiency AC/DC Converter With Quasi-Active Power Factor Correction"*IEEE Trans. Power Electron., vol. 25, no.5,May 2010.*

[2] R. Redle,L. Balogh, and N. O. Sokal,"A new family of single-stage isolated power factor correctors with fast regulation of the output voltage,*"in Proc. IEEE PESC 1994 Conf.,pp. 1137–1144.*

[3] C. Qian and K. Smedley,"A topology survey of single-stage power factor with a boost type input-current-shaper,*"IEEE Trans. Power Electron., vol. 16, no. 3,pp. 360–368, May 2001.*

[4] Oscar García, José A. Cobos, Roberto Prieto, Pedro Alou, and Javier Uceda, "Single Phase Power Factor Correction: A Survey," *IEEE Trans. Power Electronics, vol. 18, no. 3, May 2003.*

[5] T.-F. Wu, T.-H. Yu, and Y.-C. Liu, "An alternative approach to synthesizing single-stage converters with power factor correction

feature," *IEEE Trans. Ind. Electron., vol. 46, no. 4, pp. 734–748, Aug. 1999.*

[6] Heng-Yi Li, Hung-Chi Chen, "Analysis and Design of a Single-Stage Parallel AC-to-DC Converter," *IEEE Trans. Power Electronics, vol. 24, no. 12, December 2009.*

[7] L. Huber, J. Zhang, M. Jovanovic, and F.C. Lee, "Generalized topologies of single-stage input-current-shaping circuits," *IEEE Trans. Power Electron., vol. 16, no. 4, pp. 508–513, Jul. 2001.*

[8] H. Wei, I. Batarseh, G. Zhu, and K. Peter, "A single-switch AC-DC converter with power factor correction," *IEEE Trans. Power Electron., vol. 15, no. 3, pp. 421–430, May 2000.*