

# Design and Analysis of Track and Hold Circuit for high speed communication

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**Abstract:** Since the current demand for high-resolution and fast analog to digital converters (ADC) is driving the need for track and hold amplifiers (T&H) operating at RF frequencies. A very fast and linear T & H circuit is the key element in any modern wideband data acquisition system. Applications like a cable-TV or a broad variety of different radio standards require high processing speeds with high resolution. The track-and-hold (T&H) circuit is a fundamental block for analog-to-digital (A/D) converters. Its use allows most dynamic errors of A/D converters to be reduced, especially those showing up when using high frequency input signals. Having a wideband and precise acquisition system is a prerequisite for today's trend towards multi-standard flexible radios, with as much signal processing as possible in digital domain. This project is proposed to find the effect of various design schemes and circuit topology for track- and-hold circuit to achieve acceptable linearity, high speed, low power consumption, low chip area and low noise for high speed data communication. Proposed work will convert analog track and hold circuit into VLSI using mixed signal VLSI design.

**Keywords:** Track and Hold circuit, low power consumption, low chip area, sampling switch.

## I. INTRODUCTION

Track and hold circuit is the fundamental block for analog-to-digital converters(A/D). Its use allows most dynamic errors of A/D converters to be reduced, especially those showing up when using high frequency input signals. Track and hold circuit is inserted in front of a comparator array of a flash A/D converter to keep comparator's input voltages constant while the comparators are settling their output voltage levels. This Project includes different approaches for track and hold circuit.

This paper investigates effect of various design schemes and circuit topology for track-and-hold circuit to achieve acceptable linearity, high slew rate, low power consumption and low noise. Superior speed & acceptable linearity of source-followers makes it promising candidate for the purpose of this work.

## II. LITERATURE REVIEW

From the rigorous review of related work and published literature it is observed that many researchers have designed different techniques for high speed communication in different technologies. Since the real world today VLSI/CMOS very much in demand, from the careful study of reported work it is observed that track and hold circuit is the fundamental block for block for A to D converters. Its used for most dynamic errors of A to D converters to be reduced especially high frequency input signal.

A.N. Karanicolas, "A 2.7-V 300-MS/s track-and-hold amplifier," IEEE J. Solid-State Circuits, Dec,1997. In this Paper A.N. Karanicolas invented a fully differential bipolar track and hold amplifier(THA) employed an open-loop linearization technique compatible with low supply voltage. A feed through reduction method utilized the

junction capacitance of a replica switch to provide a close match to the junction capacitance of the main switch.[1]

W. Yu, S. Sen and B. H. Leung, "Distortion Analysis of MOS Track-and-Hold Sampling Mixers Using Time-Varying Volterra Series",IEEE Transactions on circuits and systems-II: Analog and Digital Signal Processing, vol. 46, No. 2, Feb.1999. In this paper time-varying theory of Volterra series is developed and applied in the sampled-data domain to solve for harmonic and intermodulation distortion of a MOS-based track-and-hold sampling mixer with a nonzero fall-time LO waveform. Distortion due to sampling error is also calculated. These results, when combined with the continuous-time solution, quantify harmonic and intermodulation distortion of a track-and-hold type mixer completely. Closed form solutions are obtained. As a practical consequence, it is shown that for certain fall-time, the distortion of track-and-hold mixers can be better than what would be predicted by a simple application of time-invariant Volterra series theory.[2]

A. Boni, A. Pierazzi, and C. Morandi, "A 10-b 185-MS/s track-and-hold in 0.35- $\mu$ m CMOS,"IEEE J. Solid-State Circuits,,Feb. 2001. This master paper described the design of a track-and-hold (T&H) circuit with 10bit resolution, 185MS/s. It is designed in a 0.35 $\mu$ m CMOS process. The circuit is supposed to work together with a 10bit pipelined analog to digital converter.[3]

Mohammad Hekmat and Vikram Garg, "Design and Analysis of a Source-Follower Track-and-Hold Circuit" , EE315 (VLSI data conversion circuits), June 2006, this paper investigates effect of various design schemes and circuit topology for track and-hold circuit to achieve acceptable linearity, high slew rate, low power consumption and low noise.[4]

Takahide SATO†a), Member, Isamu MATSUMOTO, Nonmember, Shigetaka TAKAGI, Member, and Nobuo FUJII, Fellow, “Design of Low Power Track and Hold Circuit Based on Two Stage Structure”, June 2008. In this paper, two track and hold circuits are designed and implemented using 65 nm CMOS technology. The first circuit is based on a dummy switch topology to decrease the charge injection error. The second circuit used a clock linearization technique to reduce the sampling instant inaccuracy. Simulation results showed that the track and hold circuit based on dummy transistor technique presented the best performances in terms of rapidity and accuracy.[5]

### III. PROBLEM DEFINITION

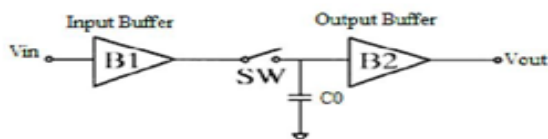
Track and hold circuit is an important block used in Analog to Digital converter in front of array comparators to keep comparators input voltage constant.

Hence to design stable track and hold circuit is main task of our project proposal. Various design schemes and circuit topology will be investigated for track and hold circuit. Track and hold circuit will be design using 32 nm CMOS technology to achieve acceptable linearity and low noise.

Today, for high speed communication circuit power consumption is important parameter. Hence the problem definition of proposed project work is to design and analyze low power, low chip area track and hold circuit applicable for high speed communication.

### IV. PROPOSED WORK

The circuit diagram of Track and Hold circuit is



**Figure: Circuit of Track and Hold circuit**

The above circuit consist input and output buffer is simply connected by sampling switch.

Track and hold circuit is a newly found fundamental circuit, whose behaviour is predicted by various design schemes and investigations of circuit topologies. Every step of design follows the design flow of Microwind 3.1 software. The design methodology will be according to VLSI design flow.

To achieve the proposed target following steps are included in the design and analysis of track and hold circuit.

- 1) Design of single MOS switch using 32 nm CMOS technology.
- 2) Design of Transmission gate using 32 nm CMOS technology.
- 3) Design of conventional track and hold circuit using source follower.
- 4) Design and analysis of track and hold circuit using transmission gate sampling switch.
- 5) Design and analysis of pseudo differential track and hold circuit

- 6) Design and analysis of fully differential track and hold circuit.
- 7) Comparison of all track and hold circuit and their analysis.

### V. CONCLUSION

In this paper, we are going to design a Track and hold circuit by using 32 nm CMOS technology to achieve acceptable linearity and low noise. Today, for high speed communication circuit power consumption is important parameter. Hence the problem definition of proposed project work is to design and analyze low power, low chip area track and hold circuit applicable for high speed communication. The purpose of this work is to design a low-power track-and-hold circuit with 32nm CMOS technology with a supply voltage of 0.8-1.2Volt.

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