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Design of 32-Bit UT Multiplier using Reversible logic and Comparison with Different Adders: A Vedic Mathematical Approach

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Abstract: Multipliers are vital components of any processor or computing machine. Performance of microcontrollers and Digital signal processors are evaluated on the basis of number of multiplications performed in unit time.To enhance speed many modifications over the standard modified booth algorithm, Wallace tree methods for multiplier design have been made and several new techniques are being worked upon. Amongst these Vedic multipliers based on Vedic mathematics are presently under focus due to these being one of the fastest and low power multiplier. Hence better multiplier architectures are bound to increase the efficiency of the system. Vedic multiplier is one such promising solution and has better results. Its simple architecture coupled with increased speed forms an unparalleled combination for serving any complex multiplication computations. Tagged with these highlights, implementing this with reversible logic further reduces power dissipation. Power dissipation is another important constraint in an embedded system which cannot be neglected. In this project we bring out a Vedic multiplier known as "Urdhva Tiryakbhayam"meaning vertical and crosswise, implemented using reversible logic, which is the first of its kind. This multiplier may find applications in Fast Fourier Transforms (FFTs), and other applications of DSP like imaging, software defined radios, wireless communications.

Keywords: Vedic Multiplier, Reversible Logic, Urdhva Tiryakbhayam, Ripple carry adder, Carry select linear adder, BEC-1 adder.

I. INTRODUCTION

The design for low power has become one of the greatest challenges in high-performance very large scale integration (VLSI) design in recent years. As a result, many methods have been introduced to minimize the power consumption of new VLSI systems.Most of these methods focus on the power consumption during normal mode of operation, while test mode operation has not normally been a predominant concern. However, it has been found that the power consumed during test mode operation is often much higher than during normal mode operation. This is because most of the consumed power results from the switching activity in the nodes of the circuit under test (CUT), which is much higher during test mode than during normal mode operation [1].Vedic mathematics is the ancient Indian system of mathematics which mainly deals with Vedic mathematical formulae and their application to various branches of mathematics. Vedic mathematics was reconstructed from the ancientIndian scriptures (Vedas) by Sri Bharati Krishna Tirtha after his research on Vedas.

He constructed 16 sutras and 16 upa sutras after extensive research in Atharva Veda. The most famous among these 16 are Nikhilam Sutram, Urdhva Tiryakbhayam, and Anurupye. It has been found that Urdhva Tiryakbhayam is the most efficient among these. The beauty of Vedic mathematics lies in the fact that it reduces otherwise cumbersome looking calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Hence multiplications in DSP blocks can be performed at faster rate. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering.

Digital signal processing (DSP) is the technology that is omnipresent in almost every engineering discipline. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another.
Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Trans forms etc. With ever increasing need for faster clock frequency it becomes imperative to

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have faster arithmetic unit. Hence Vedic mathematics can be apply employed here to perform multiplication.

Vedic Mathematics offers a fresh and highly efficient approach to mathematics covering a wide range - starts with elementary multiplication and concludes with a relatively advanced topic, the solution of non-linear partial differential equations. But the Vedic scheme is not simply a collection of rapid methods it is a system, a unified approach. Vedic Mathematics extensively exploits the properties of numbers in every practical application. The objective of good multiplier to provide a physically compact high speed and low power consumption unit. Being a core part of arithmetic processing unit, multipliers are in extremely high demand on its speed and low power consumption.

To reduce significant power consumption of multiplier design it is a good direction to reduce number of operations there by reducing a dynamic power which is a major part of total power dissipation. In the past considerable effort were put into designing multiplier in VLSI in this direction Reversible logic is one of the promising fields for future low power design technologies. Since one of the requirements of all DSP processors and other hand held devices is to minimize power dissipation multipliers with high speed and lower dissipations are critical.

This paper proposes an implementation of Reversible Urdhva Tiryakbhayam Multiplier which consists of two cardinal features. One is the fast multiplication feature derived from Vedic algorithm Urdhva Tiryakbhayam and another is the reduced heat dissipation by the virtue of implementing the circuit using reversible logic gates. The paper is partitioned into six sections. Section II gives literature survey, Section III deals with reversible logic. Section IV explains the Urdhva Tiryakbhayam algorithm. Section V elaborates on the design aspects of Reversible Urdhva Tiryakbhayam Multiplier. Section VI Conc1usions and references follow.

II. LITERATURE SURVEY

Energy loss is an important consideration in digital circuit design.A part of this problem arises from the technological non ideality of switches and materials. The other part of the problem arises from Landauer's principle for which there is no solution. Landauer's Principle states that logical computations that are not reversible necessarily generate k*T*ln(2) joules of heat energy, where k is the Boltzmann's Constant k=1.38x10-23 J/K, T is the absolute temperature at which the computation is performed[3]. Although this amount of heat appears to be small, Moore's Law predicts exponential growth of heat generated due to information lost, which will be a noticeable amount of heat loss in next decade. showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way also by second law of thermodynamics any process that is reversible will not change its entropy On thermo dynamical grounds, the erasure of one bit of information from the mechanical degrees of a system must be accompanied by the thermalization of an amount of k*T*ln (2) joules of energy. The information entropy H can be calculated for any probability distribution. Similarly the thermodynamic entropy S refers to thermodynamic probabilities specifically. Thus gain in entropy always means loss of information, and nothing more

Design that does not result in information loss is called reversible. It naturally takes care of heat generated due to information loss. Bennett showed that zero energy dissipation would be possible only if the network consists of reversible logic gates, he showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way[4] Thus reversibility will become an essential property in future circuit design technologies

III. REVERSIBLE LOGIC

Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in dose proximity. The basic principle of reversible computing is that a bijective device with an identical number of input and output lines will produce acomputing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state,resulting in no heat dissipation [3].

A reversible logic gate is an N-input N-output logic device that provides one to one mapping between the input and the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. Garbage outputs are those which do not contribute to the reversible logic realization of the design.Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. Gate count is the number of reversible gates used to realize the function. Gate level refers to the number of levels which are required to realize the given logic functions [2].

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The following are the important design constraints for reversible logic circuits.
1. Reversible logic gates do not allow fan-outs.
2. Reversible logic circuits should have minimum quantum cost.
3. The design can be optimized so as to produce minimum number of garbage outputs[5]
4. The reversible logic circuits must use minimum number of constant inputs [5].
5. The reversible logic circuits must use a minimum logic depth or gate levels.

The basic reversible logic gates encountered during the design are listed below:

1. Feynman Gate :

It is a 2x2 gate and its logic circuit is as shown in the figure 1. It is also known as Controlled Not (CNOT) Gate. It has quantum cost one and is generally used for Fan Out purposes.[6]

2. Peres Gate (PG):

It is a 3x3 gate and its logic circuit is as shown in the figure 2. It has quantum cost four. It is used to realize various Boolean functions such as AND, XOR[7]

3. Fredkin Gate:

It is a 3x3 gate and its logic circuit is as shown in the figure 3. It has quantum cost five. It can be used to implement a Multiplexer [6].

4. Double Peres Gate (DPG):

This is one of the four input Reversible logic Gate is shown in figure 4.which can be used as full-adder. The full adder using DPG is obtained with C=0 and D= Cin and its quantum cost is equal to 6.

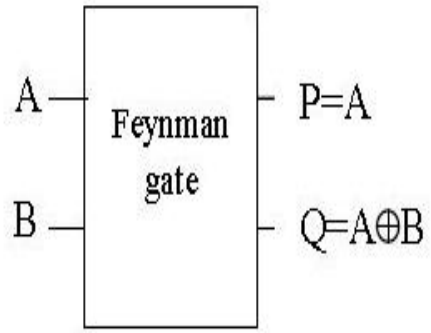

Fig 1.logic circuit of Feynman gate

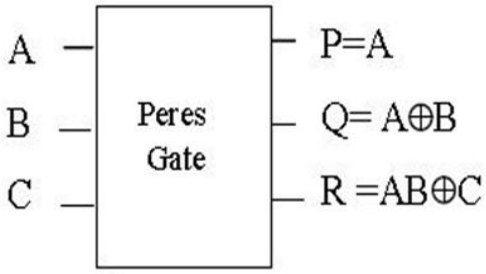

Fig 2.logic circuit of Peres gate

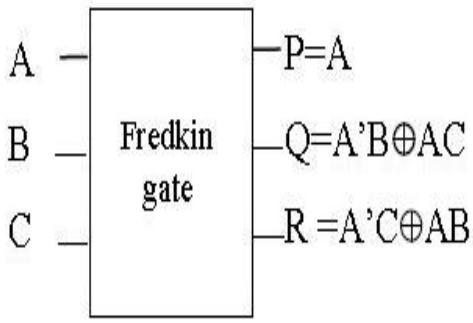

Fig 3.logic circuit of Fredkin gate

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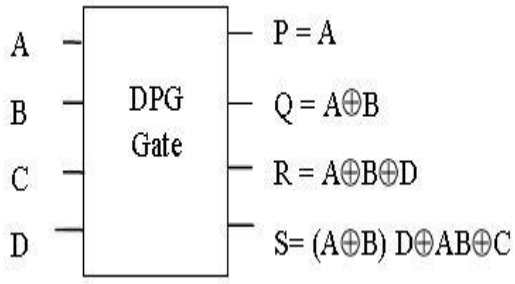

Fig 4.logic circuit of DPG gate

IV. URDHVA TIRYAKBHAYAM MULTIPLICATION ALGORITHAM

Urdhva Tiryakbhayam (UT) is a multiplier based on Vedic mathematical algorithms devised by ancient Indian Vedic mathematicians. Urdhva Tiryakbhayam sutra can be applied to all cases of multiplications viz. Binary, Hex and also Decimals. It is based on the concept that generation of all partial products can be done and then concurrent addition of these partial products is performed.

The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhayam. Unlike other multipliers with the increase in the number of bits of multiplicand and/or multiplier the time delay in computation of the product does not increase proportionately. Because of this fact the time of computation is independent of clock frequency of the processor. Hence one can limit the clock frequency to a lower value Also, since processors using lower clock frequency dissipate lower energy, it is economical in terms of power factor to use low frequency processors employing fast algorithms like the above mentioned. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases at a slow pace as compared to other conventional multipliers.The algorithm can be illustrated using the following visual walkthrough in the below figure5.

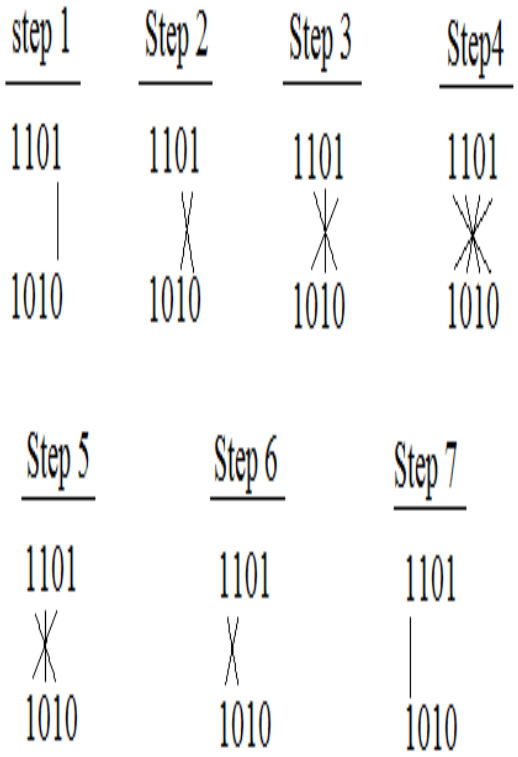

Fig.5 Using Urdhva Tiryakbhayam for binary numbers

V. ARCHITECTURE OF REVERSIBLE URDHVA TIRYAKBHAYAM MULTIPLIER

Implementation of 2x2 UT multiplier using reversible logic gate

A 2 x 2 Urdhva Tiryakbhayam Multiplier using reversible logic gates can be implemented based on the logical expressions obtained while designing the 2 x 2 UT Multiplier using the conventional logic gates.

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In designing the 2 x 2 UT Multiplier using reversible logic gates we use three fundamental reversible gates namely, PERES Gate(PG) , FEYNMAN Gate(which is also termed as control NOT Gate(CNOT Gate)) [9] is as shown in figure 6.

The Peres Gate can be used as half-adder by making the third input as logic zero(C=0). The sum and the carry of the half-adder are obtained on the third and fourth pins of the Peres Gate. The CNOT Gate is used to generate the Ex-or product of the two inputs

- The circuit requires a total of six reversible logic gates out of which five are Peres gates and remaining one is the CNOT gate.The quantum cost of the 2x2 UT Multiplier is enumerated to be 21.
- The number of Garbage outputs is 9 and the number of Constant inputs is 4.
- This 2x2 multiplier block is cascaded to obtain 4x4 multiplier.

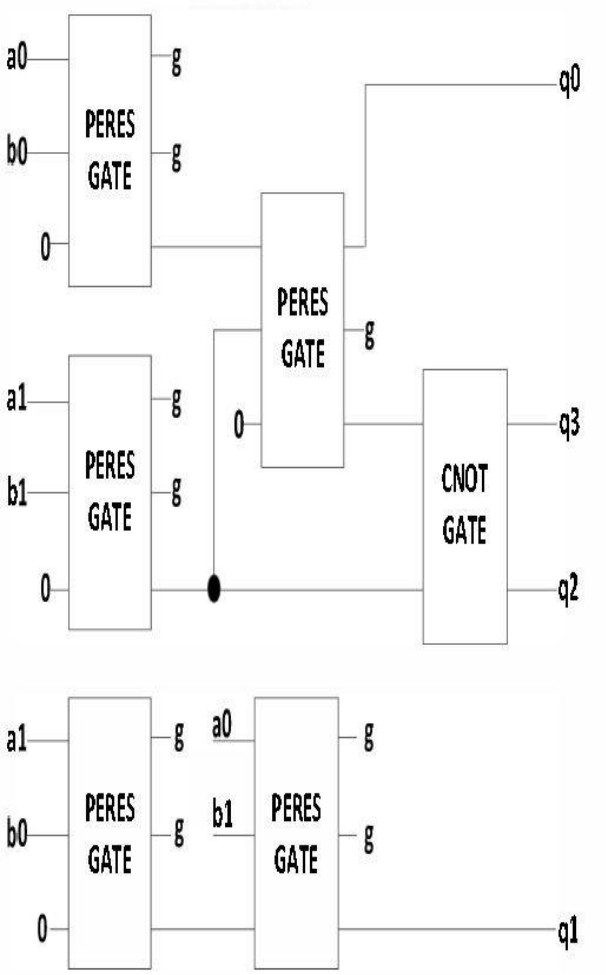

Fig. 6 Reversible implementation of 2x2 UT Multiplier

4-Bit Ripple carry adder using reversible gates

In implementing 4 x 4 Urdhva Tiryakbhayam Vedic Multiplier using Reversible Logic Gates we require to implement the 4-bit parallel adder for the addition of partial products, which are generated intermediately.Thus a 4 bit ripple carry adder needs 4 DPG gates and the 5 bit adder requires 5 DPG gates is shown in figure 7. This design also does not take into consideration the fan out gates [1]

Here, in designing the 4-bit parallel adder we make use of Peres Gate (PG) and Double Peres Gate (DPG) to generate the sum. The Peers Gate(PG) is used as half-adder by making the third input as logic zero (C = 0), While the carry generated in present stage is propagated to the next stage as in case of ripple carry adder and the propagated carry is considered as third input to the full-adder. The Double Peres Gate (DPG) is used as full-adder to add the three bits (including the carry generated in the previous stage) and it is used as full-adder by making the third input as logic zero (C = 0) to generate the carry of that stage by adding three bits in that stage (including the carry generated in the previous stage)

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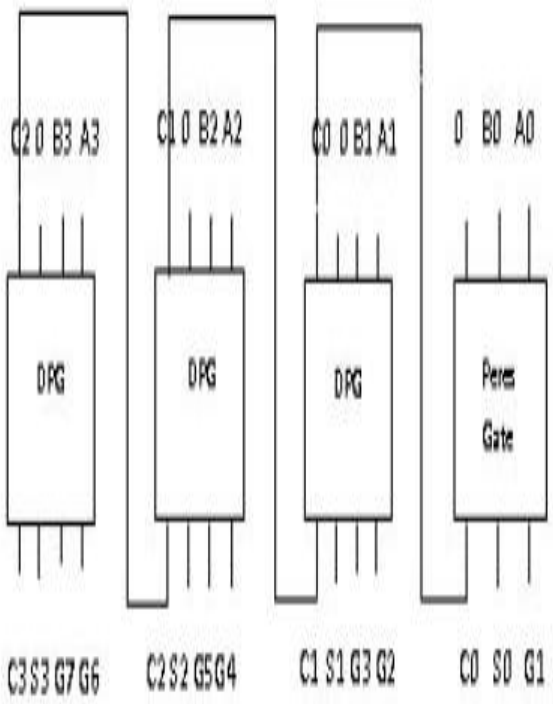

Figure7: 4-Bit Ripple Carry (RC) Adder using DPG and PG gates.

Design of a 32×32 Multiplier using Ripple carry adder.

Succeeding the design of 2*2 and 4*4 Vedic Multiplier and using it as a basic building block for design of 4 * 4 bit Vedic Multiplier. This is done by adding partial products using adders. Then by using 4*4 bit Vedic Multiplier as a building block, 8*8 bit Vedic Multiplier have been designed.

By using this 8*8 bit Vedic Multiplier16*16 bit Vedic Multiplier is designed and then finally 32*32 bit Vedic Multiplier is designed as shown in figure 8.

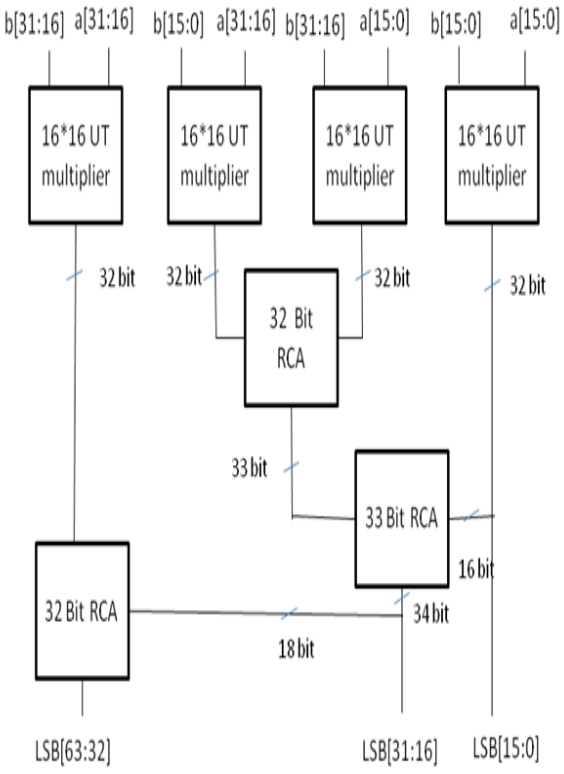

Fig:8 :32bit multiplier using Ripple carry adders.

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Carry Select Linear Adder:

A Carry Select linear Adder (CSLA) is a modified adder used in place of RCA to reduce delay. In CSLA the total number of bits to be added is divided in to two halves which are of equal size as show in figure 9. In stage-1 the first half of the bits are added as in RCA and the remaining bits are added by assuming the carry input to be o and 1 in stage 2 and 3 respectively. Here the outputs from stage 2 and 3 are generated at once and these are given as inputs to a 2:1 multiplexer with carry as selection line.

The carry-select linear adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry-in being zero and the other assuming it will be one. After the two results are calculated, the correct sum, as well as the correct carry-out, is then selected with the multiplexer once the correct carry-in is known.

In CSLA the results from stages 1, 2 and 3 are generated at the same time so that total delay is greatly reduced.

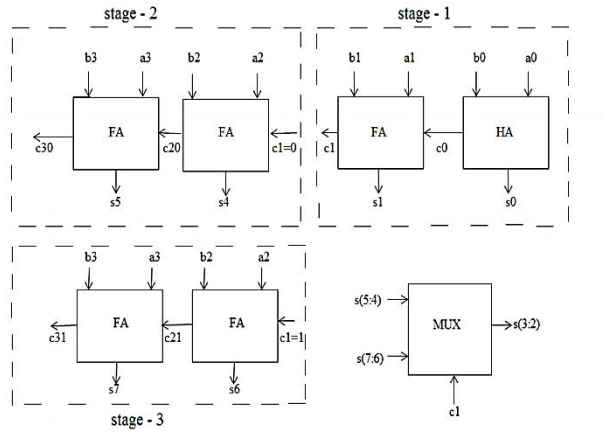

Fig 9. Carry select adder for 4 bit

Design of a 32×32 Bit Multiplier using carry select linear adder

The first step in the design of 32×32 block will be grouping the 16 bit (byte) of each 32 bit input. These lower and upper bytes pairs of two inputs will form vertical and crosswise product terms. Each input byte is handled by a separate 16×16 Vedic multiplier to produce 32 partial product rows.

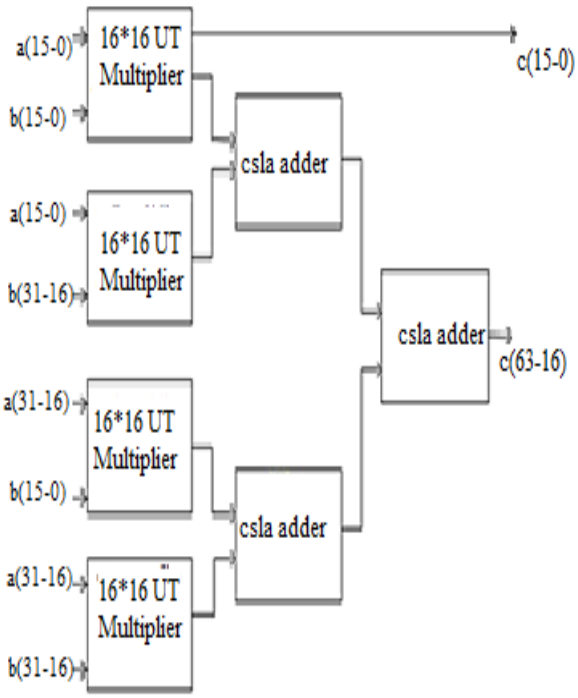

Fig:10 :32 bit multiplier using CSLA adder

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These partial products rows are then added in a carry select adder optimally to generate final product bits. The figure 10 shows the schematic of a 32×32 block designed using 16×16 blocks. The partial products represent the Urdhva vertical and cross product terms. Then using or and half adder assembly to find the final product [8]

Binary to excess-1 converter:

The basic work is to use Binary to Excess-1 Converter (BEC) in the regular CSLA to achieve lower area and increased speed of operation. The main advantage of this BEC logic comes from the fact that it uses lesser number of logic gates than the n-bit Full Adder (FA) structure. The structure of a 5-bit BEC is shown in Fig

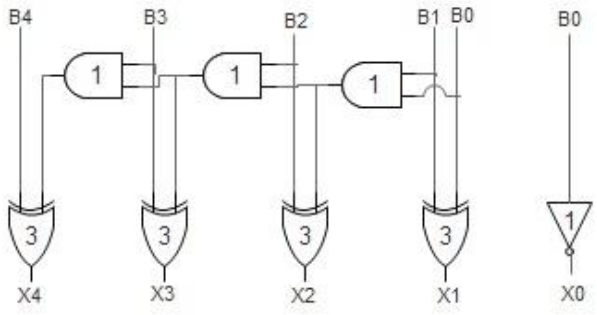

Fig 11. Binary to Excess-1 Converter for 5-bit.

Design of 32*32Multiplier using BEC adder

A Binary to Excess-1 Code Converter Adder is a modified CSLA is shown in figure 12. BEC-1 will increment the given inputs by one. By this BEC-1 adder efficient area and delays can be achieved for the multipliers. These BEC adders are preferred to achieve a multi-trade off among delay and memory. The delay and memory of a multiplier is totally based on the type of adders implemented in it. By using conventional full and half adders we cannot achieve efficient values in delay and memory .By replacing these adders with BEC structure a lot of memory can be saved .In similar fashion delay can also be greatly reduced [10] This architecture contains 4 blocks of equal size i.e. each block consists of 16x16 Vedic Multiplier whose inputs are partitioned according to Urdhva-Tiryagbhyam sutra. Outputs from Vedic Multiplier are given as inputs to BEC adders.

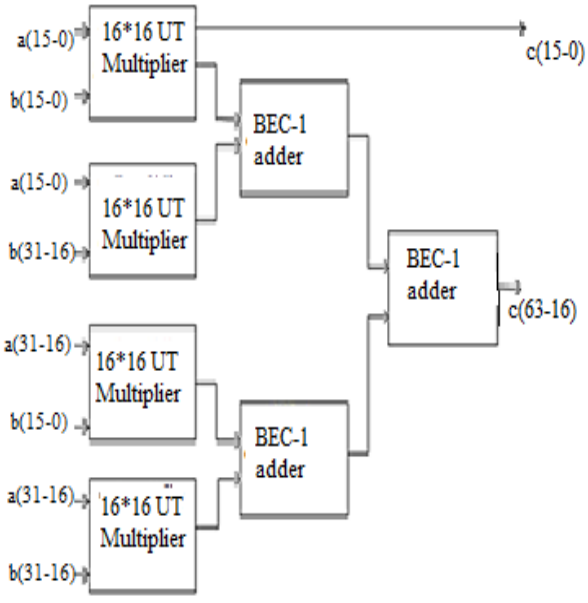

Fig:12 :16 bit multiplier using BEC adder

VI. RESULTS

The Input output waveforms which are generated by using XILINX software and device utilization summary are shown in figure 13 and table 1.

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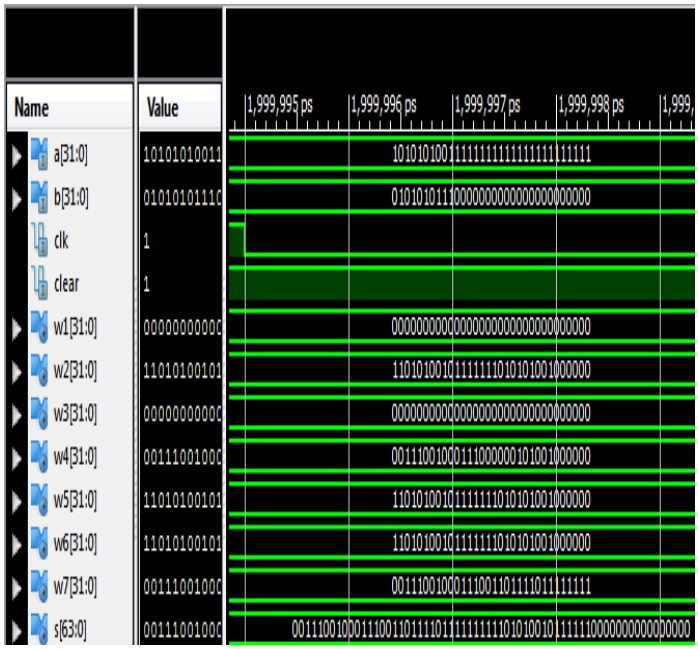

Fig 13. Simulation results for 32 Bit UT Multiplier using reversible logic

Table 1:Device utilizationsummary for 32 bit vedic multiplier using reversible logic gates with different adders.

Logic utilization	32*32 vedic multiplier using RCA adder	32*32 vedic multiplier using CSLA adder	32*32 vedic multiplier using BEC adder	32*32 vedic multiplier using Reversible logic gates
No.of slice register	1813	783	1816	1734
NO.of LUT' s	3156	4223	3631	3085
No.of IOB' s	128	130	130	130
Memory in (KB)	381312 KB	430208 KB	444992 KB	438464 KB
Delay in (ns)	83.31ns	56.03ns	73.42ns	70.19ns
Power(mw)	100.82mw	99.2mw	101.53mw	97.91mw

VII. CONCLUSION

The main aim of UT algorithm with reversible logic is to design low power multipliers. This is the optimized design as compared to vedic multiplier using basic logic gates. By using this reversible logic gates power utilization is reduced compared to the basic logic gates.The result of carry select adder is improvements over delay than other adders. The further optimization of the circuit in terms of high speed and low power as future work.

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