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Phase Frequency Detector in Phase Lock Loop

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Abstract: Industry is approaching towards complete system-on-chip (SoC) design solutions that include power management. Power has become one of the most important part of design convergence for multi gigahertz communication systems such as optical data links, wireless products, microprocessor & ASIC/SOC designs. Hence by using 45nm CMOS technology parameters PLL is designed. This gives at low power consumption high speed performance. MOS model called BSIM4 recommended for ultra-deep submicron technology simulation. The Software Tanner13.0 tool used to allows designing and simulating an integrated circuit at physical description level. Today's communication systems, processors and computing devices require circuit of low power consumption, small size, high speed and low fabrication cost for these requirements to design PLL by using 45nm CMOS technology. The main objective of PLL is to generate signal in which phase of feedback signal is same as phase of reference signal. This is achieved after many iteration of comparison of the reference and feedback signal. One of them is XOR gate based detection but it is less preferred as compared to the PFD. The reason behind rejecting use of XOR gate as detector was that that it can lock onto harmonics of the reference signal and most important it cannot detect a difference in frequency. These disadvantages were overcome by other type of PFD.

Keywords: Phase Lock Loop (PLL), Phase Frequency Detector (PFD), 45nm CMOS Technology, Tanner13.0

I. INTRODUCTION

With the fast development of CMOS technology, so many signal processing functions are implemented in the digital domain for low cost, low power consumption and high speed. PLL is a modern electronics as well as communication system. Recently ample of researches have conducted on the design of PLL circuit and still research is going on this topic. Most of the researches have conducted to recognize a higher lock range PLL with lesser lock time and have tolerable phase noise. PLL are used for clock generation and clock recovery in microprocessor, networking and communication systems. PLLs are used to generate well-timed on-chip clocks in high-performance digital systems. Modern wireless communication systems make use of PLL mainly for skew and jitter reduce PLL locate wide application in several modern applications mostly in advance communication and instrumentation systems. PLL is a mixed signal circuit involves design challenge at high frequency. Presently almost all communication and electronics devices operate at a higher frequency, so for that purpose we need a faster locking PLL. So there are a lot of challenges in designing the mentioned different blocks of the PLL to operate at a higher frequency. And these challenges motivated towards this research topic. In this work mainly the faster locking of the PLL is concentrated by properly choosing the PFD circuit architectures and parameters. Today's communication systems and computing devices require circuit of low power consumption, small in size, high speed and low fabrication cost. We are going to design the PFD with the help of CMOS technology that will solve the problem of power consumption, area consumption and generate the desired frequency band.

II. DESIGN AND SYNTHESIS OF PFD

Phase Frequency Detector is most important part in Phase Lock Loop. PFD compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency variation, it generates two output signals "UP" and "DOWN". Figure1 shows a traditional PFD circuit. If there is a phase difference between the two signals, it will generate "UP" or "DOWN" synchronized signals. When the reference clock rising edge leads the feedback input clock rising edge "UP" signal goes high while keeping "DOWN" signal low. On the other hand if the feedback input clock rising edge leads the reference clock rising edge "DOWN" signal goes high and "UP" signal goes low. Fast phase and frequency acquisition PFDs are generally preferred over traditional PFD.

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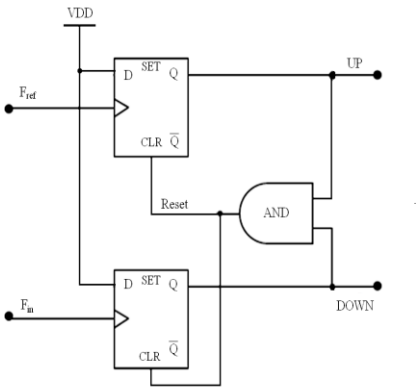

Fig.1. Block diagram of traditional PFD circuit [1]

The schematic level design entry of the circuits is carried out in the Tanner13.0 tool Design Environment. The layout of the PLL is designed in L-Edit of Tanner13.0 using 45nm CMOS library. In order to analyze the performances, these circuits are simulated in the S-Edit of Tanner13.0 tool. Different performance indices such as phase noise, power consumption and lock time are measured in this environment. Transient, parametric sweep and phase noise analyses are carried out in this work to find out the performances of the circuit. The optimization of the PFD the scale factor for transistor sizing is found out using the calculations of parameters selecting from 45nm CMOS library. Since PFD is the heart of the whole PLL system, it should be designed in a proper manner. The design steps for the PFD are as follows.

Step 1:
Drain current in saturation region is,

$$I_D = \frac{1}{2}\mu_n Co_x \frac{W}{L}\left(V_{gs} - V_{in}\right)^2 \qquad (1)$$

Step 2:
From above Drain current equation, find the width of CMOs Transistor by using following formula,

$$W = \frac{2I_D L}{\mu_n Co_x \left(V_{gs} - V_{ijn}\right)^2} \qquad (2)$$

Where,

I_D=Drain current,
Co_x =Oxide capacitance in F/m^2

Step 3:
The value of Oxide Capacitance is unknown, for finding the value of Co_x use following formula,

$$Co_x = \frac{\varepsilon_o k}{To_x} \qquad (3)$$

Where,
ε_0=Relative Permittivity Constant = 8.85×10^{-12} F/m
k=Dielectric constant of dielectric material used as gate oxide
To_x= Gate oxide thickness

Step 4:
Choose gate oxide Hafnium Oxide (HfO_2) because HfO_2 the surface absorb higher amounts of moisture and bind moisture than Silicon Oxide (SiO_2). So that HfO_2 chooses 4-6 time higher than SiO_2. Also the value of V_{gs} and V_{in} select from 45nm CMOs model file.

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Table 1. PFD design specifications

Parameters	Definition	Value
V_{DD}	V_{DD}	1 V
To_x	Gate Oxide Thickness	1.75 nm
Gate dielectric	Gate dielectric	SiO_2, HfO_2
W	Width	160.94nm
L	Length	45nm
Co_x	Oxide capacitance	0.11 f/m^2

III. SIMULATION RESULT

Phase Frequency Detector is most important part in Phase Lock Loop. For implementation of PFD CMOS transistor, two D flip flop, AND gate and NOT gate are used as shown in figure2. D flip flop reset by using AND and NOT circuitry. There are two input frequencies Fref and Fin. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals “UP” and “DOWN”.

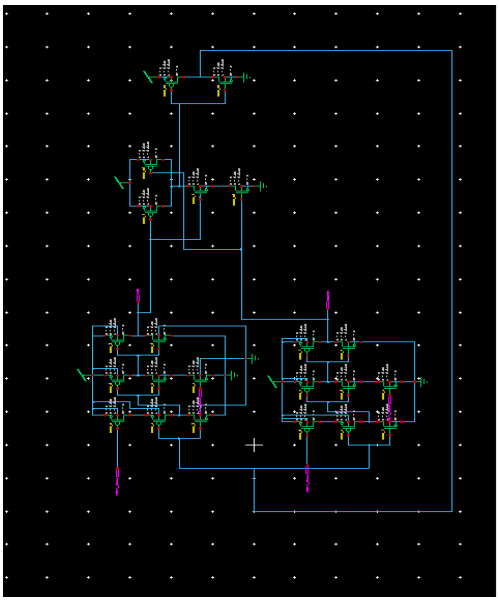

Fig.2. Circuit diagram of DFF PDF

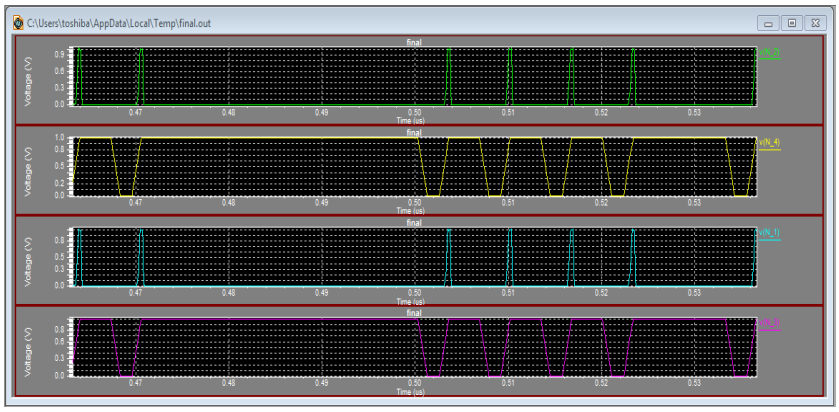

Fig.3. Result of PFD when same frequency apply to Fref and Fin

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When there is phase difference between reference clock and feedback clock the PFD gives output as error on "UP" and "DOWN" clock. PFD compares the phase and frequency difference between the reference clock and the feedback clock which is the first and most important step towards rectification of the phase difference. If there is no phase difference, PFD gives same signal at output and hence it reduces the locking time. When we apply same pulse width = 6.6ns and period = 3.3ns to feedback clock (v(N_1)) and reference clock (v(N_3)) it gives same signal on "UP"(v(N_2)) and "DOWN" (v(N_4)) clock as shown in figure3. The locking time for same frequency is 5.0ns.

IV. CONCLUSION

A PLL is a closed-loop feedback system that sets fixed phase associate between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase changes that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock to produce a high-frequency clock this is known as clock synthesis. In this work, the PLL has been successfully designed and simulated using S- Edit of Tanner13.0 EDA tool at 45nm CMOS technology. In this work PFD designed for 1GHz frequency at 1V. The main motive of this work is to check the locking time for same frequency. In this work a PFD with a better lock time is presented. The lock time of the PFD is found to be 5.0 ns. The PFD circuit consumes a power of 45 W from a 1 V D.C. supply. The lock time of the PLL mainly depends upon the type of PFD architecture used and the parameters of the transistor and DFF. So by properly choosing the PFD architecture and adjusting the CMOS component values a better lock time can be achieved. The centre frequency of oscillation of the VCO depends upon the sizing of the transistors. To reduce transistor size choose proper frequency deviation from desired value.

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REFERENCES

[1] Z. Song, X. Liu, X. Zhao, Q. Liu, Z. Jin, and B. Chi, "A Low-Power NB-IoT Transceiver With Digital-Polar Transmitter in 180-nm CMOS," IEEE Transactions on circuits and systems, May 15, 2017.
[2] A. Shivhare, M. Gupta, "Low Power Ring Oscillator at 180nm CMOS Technology," International Journal of Computer Application, ISSN: 0975 – 8887 Volume 144 – No.8, June 2016.
[3] P. Sreehari, P. Kumarsharma, D. Palli, D. Kewale, O. Asbe, K. Prasad, "Power Optimized PLL Implementation in 180nm CMOS Technology," IEEE Conference, 2014.
[4] N. Pathak, R. Mohan, "Performance Analysis and Implementation of CMOS Current Starved Voltage Controlled Oscillator for Phase Locked Loop," International Journal of Emerging Technology and Advanced Engineering ISSN 2250-2459, ISO 9001:2008 Certified Journal, Vol. 4, Issue 3, March 2014.
[5] A. Khode, M. Mahendra, "Efficient Wide Frequency Range Voltage Control Oscillator for PLL using 180nm CMOS Technology," International Journal of Engineering Research & Technology, ISSN: 2278-0181 Vol. 4 Issue 06, June-2015.
[6] A. Agrawal, R. Khatri, "Design of Low Power, High Gain PLL using CS-VCO on180nm Technology," International Journal of Computer Applications, Vol. 122 – No.18, July 2015.
[7] M. Mansuri, D. Liu, and C.Yang, "Fast Frequency Acquisition Phase Frequency Detector for G Samples/s Phase Locked Loops," IEEE Journal of Solid State Circuit, Vol. 37, No. 10, October 2002.
[8] S. Li, and H. Hsieh, "A 10 GHz Phase-Locked Loop with a Compact Low-Pass Filter in 0.18 μm CMOS Technology," IEEE Microwave and Wireless Components Letters, Vol. 19, NO. 10, October 2009.
[9] A. Arakali, S. Gondi, and P. Hanumolu, "Analysis and Design Techniques for Supply- Noise Mitigation in Phase-Locked Loop,s" IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 57, No. 11, November. 2010.