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Modified GDI technique for low power and high efficient adders using 0.13µm technology

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Abstract-Gate Diffusion Input-(GDI) is a novel technique for low power digital VLSI circuits to reduce the powerdissipation, propagation delay and transistor count thereby reducing the size and the area occupied by the circuit on the chip. The conventional GDI technique suffers from the voltage degradation problem. This paper presents a modified version of the GDI technique where a strong logic 1 as well as strong logic 0 is obtained. Using the Modified-GDI technique adders like RCA along with fast adders such as Carry Skip adder and Carry Look Ahead adders are built and simulated using 130nm technology. The results obtained for the Modified GDI based adders are compared with the conventional Complementary CMOS RCA, CSA and CLA adders. It is found that using the Modified GDI technique there is a significant (i.e. 45%) reduction in the power dissipation for basic 4-bit CLA adder, along with reduction in the transistor count and less propagation delay (i.e. 20%) in the RCA when using GDI Technique. The simulation is carried out in the Electric Software and LT-Spice VLSI EDA CAD tool with SPICE BSIM3 model file.

Keywords: CMOS, GDI, M-GDI, RCA, CSA,CLA

I. INTRODUCTION

The advancements in the area of Digital Signal Processing have given rise to necessity of the portable digital devices to improve the quality of the life. With this ever growing demand, the exigency is high speed, small size and lower power dissipation in the digital circuits, which are the back bone of the DSP processors. The performance of the DSP processor largely dependent upon the basic adder cells, as they take significant time for the computation of result. Hence to design a better architecture for the basic adder blocks one must reduce the delay, power consumption and area occupation in the layout. So many fast addition techniques are developed and tested. Carry Skip adder and Carry Look Ahead adders are the fastest compared to the other adders.

As one looks to improve the speed of the addition in these adders there is a significant trade off in hardware that is used in achieving this, thereby increasing the area occupied on the chip along with total powers dissipation.

Till recent, conventional CMOS technology was being used to implement the CSA and CLA to achieve speed of addition and to improve the performance of the digital circuitry. But it has become obsolete off late and Gate Diffusion Input-(GDI) technology came into picture. As the technology shrinks, though size of the transistor reduces, there should be new methodology to reduce the transistor count along with reduced power dissipation by the digital circuits.

GDI-technology is better option over Conventional CMOS in which the number of transistor used to implement a function is reduced along with the reduced overall power dissipation of the digital circuitry. It is found that GDI technique also speeds up implementing the function compared to the CMOS technology.

One of the major drawbacks of the GDI technique is degraded voltage swing i.e. in the conventional GDI a weak logic 1 as well as weak logic 0 is found at the output. Though it is acceptable in system where there less importance to the noise margin or in systems which employee additional circuitry to improve the result. Modification in the basic GDI cell its-self is a better option to achieve the full voltage swing. In this paper a Modified GDI technique is proposed for the simulation of various adders such as ripple carry adder also fast adders such as Carry Skip adder and Carry Look Ahead adders. The results are compared against the CMOS adders.Modified GDI technology is suitable for the design of fast, low power circuits using reduced number of transistors, more importantly, with full voltage swing.

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II. Basic concepts of GDI and previous work

The Basic cell structure of the GDI is as shown in the Fig 1. It is a CMOS structure and has four terminals, i.e. G (NMOS and PMOS gate are shorted), P (source of PMOS), N (Source of NMOS), Out (Drains of NMOS and MOS are tied together). The bulks of the bothNMOS and PMOS are connected to N or P. [1].

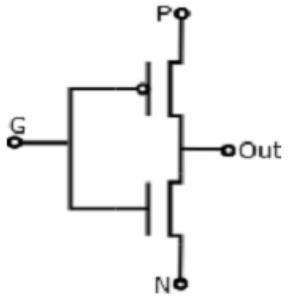

Fig 1: Basic GDI Cell consisting of PMOS and NMOS

It must be noted that, not all the functions are possible in
Standard P-Well CMOS process, but can be successfully
Implemented in Twin-Well CMOS or SOI technologies [2]. Using only two transistors multiple Boolean functions can be implemented using GDI cell and it isshown in the table1

Table 1: Boolean function synthesis through input configuration of a simple GDI Cell

N	P	G	Out	Function
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}+B$	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
0	1	A	$\bar{A}$	NOT

If the same function in the table 1 were to beImplemented in conventional CMOS technique it is fairlycomplex and would take 6 to 12 transistors. But in the GDI technique it takes only two transistors. XOR andXNOR functions are key features, while implementingthe adders and its schematic in GDI is shown in the Fig:2

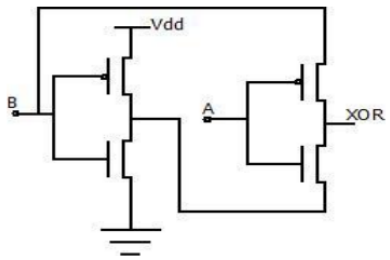

Fig 2: GDI based XOR Cell

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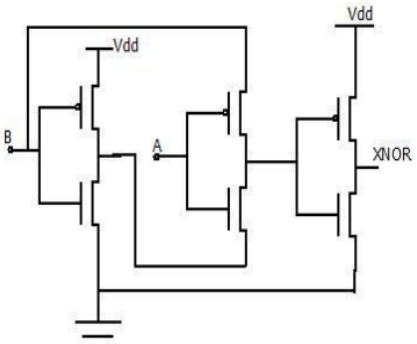

Fig 3: GDI based XNOR Cell

One can notice from the Fig 3 that in GDI using only 6 transistors XNOR function can be realised, whereas in CMOS technique 12 transistors are required. So it is obvious that using GDI, the number of transistors can it reduced significantly in adder circuit. As the number of transistors are reduced the area needed to implement the transistors are reduced to a great extent, minimizing the size of the adder on silicon. Reduction in the transistor count also reduces the powers dissipation of the circuit, so the GDI based circuits is also going to reduce the heating of the GDI block compared to CMOS based circuits. Parasitic plays a very important role in the propagation delay. As one need fast and power efficient digital circuits, in GDI since less number of transistors are utilised compared to CMOS the total propagation delay is going to be less over CMOS. So GDI technique is seen as a better option than CMOS for full custom digital circuit design.

A. Carry Look Ahead Adder

Carry look ahead adder is the most efficient adder in terms of speed while adding large number of bits. In normal ripple carry adder the next adder block needs to wait until the present FA calculates the carry, for example for a 4-bit RCA shown in Fig 4, S3 can be calculated only when C2 has arrived. The sum S2 is calculated only after s1 is arrived and so on.

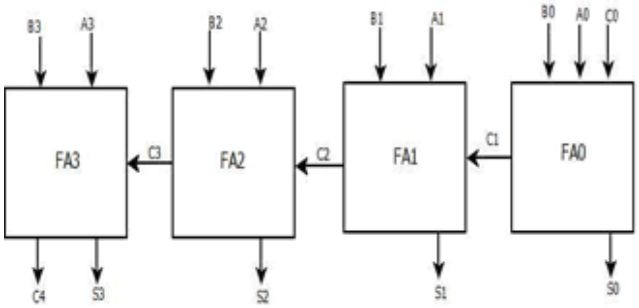

Fig 4: 4-Bit Ripple Carry Adder

CLA makes use of generate and propagate function to predict the next carry as shown in eq(1) and eq(2)

Generate, Gi = Ai AND Bi---------- (1))

Propagate, Pi = Ai XOR Bi---------- (2)

So to the sum and the next carry is calculated as

Sum, Si = Pi XOR Ci---------- (3)

Carry, Ci+1 = Gi = PiGi---------- (4))

In CLA unlike RCA need not wait for the next black to generate the carry. The sum of all the blocks are calculated simultaneously since the carry prediction has achieved using Gi and Pi function. Logic diagram of 4-bit CLA is shown in Fig 5.

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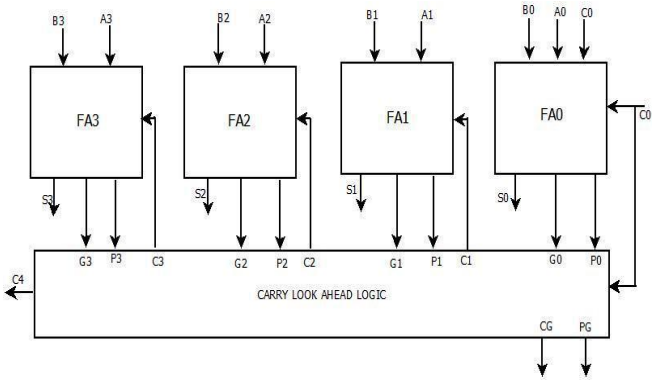

Fig5: 4-bit Carry Look Ahead Adder

II. PROPOSED MODIFIED GDI CELL BASED LOGIC GATES.

XOR gate plays a very important role in the adder circuit, as it is responsible for the generation of the sum. Building an efficient XOR results in obtaining an efficient full adder block. The basic XOR cell using GDI cell is shown in Fig 2. Where one can notice that there is a problem of voltage degradation. It is seen, When the input A= "0" and B= "0" the transistors M1 and M3 are ON and the value B="0" passes through M3, instead of "0" it will transfer V_{TP} because P-transistor transfers strong logic "1" and weak logic "0". When input A= "1" and B= "0" the transistors M1 and M4 are ON and the expected output is VDD but it will transfer V_{DD}-V_{TN} because N-transistor transfer weak logic "1" and strong logic "0". Output for the input combinations are shown in the table 2.

Table 2: GDI XOR Output

A	B	OUTPUT
0	0	V_{TP}
0	1	V_{DD}
1	0	V_{DD}-V_{TN}
1	1	0

Voltage swing degradation is a concern in the implementation of digital logic because this degradation causes the noise margin to be reduced in the overall circuit. If logic restoration is not achieved then the circuit result is going to be erroneous.Voltage swing degradation is a concern in the implementation of digital logic because this degradation causes the noise margin to be reduced in the overall circuit. If logic restoration is not achieved then the circuit result is going to be erroneous.There are various methods to restore the logic levels. One can pass the output through a pair of inverters, as shown Fig 6

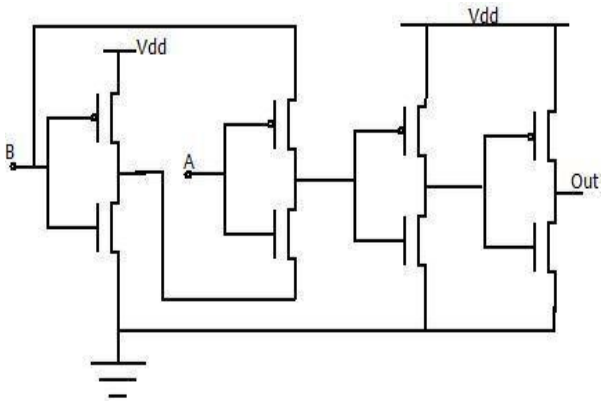

Fig 6: Swing restoration logic for GDI XOR cell

In doing so will increase the transistor count by four per cell. As the number of transistors increases, it will lead to increase in delay, increase in the power dissipation. So a better alternative is modified GDI cell for XOR gate is proposed in the below Fig 7.

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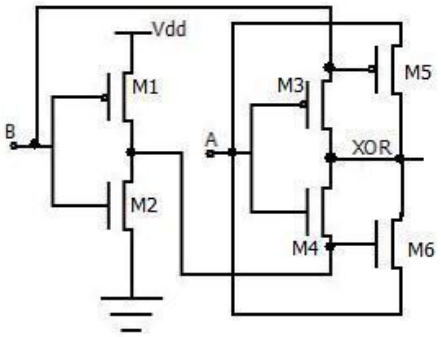

Fig 7: Modified GDI XOR cell

Here when A=B=0, M1 and M3, M5, M6 are ON, what the voltage V_{TP} was seen in the basic GDI XOR is grounded by the M6 transistor. So a perfect logic 0 is obtained at the output.
When A=1 and B=0, M1, M4, M5 AND M6 are ON, and transistor M5 is making sure that, the voltage at the output is logic 1. Hence these two addition transistors make sure that, a full swing is achieved by the XOR gate as compared to the traditional GDI cell. Even though on the outset it seems to be seen as 2 transistors are increased in number, one can achieve full swing at the output. And this structures it better than adding back to back inverters at the output of the XOR gate as shown in the Fig 7. The construction of OR as well as AND gate are also realised using the Modified GDI based cell. Hence a strong logic 0 as well as strong logic 1 is obtained at the output.

A. RCA USING MODIFIED GDI CELL

The basic XOR gate structure using Modified GDI cells are constructed as shown below

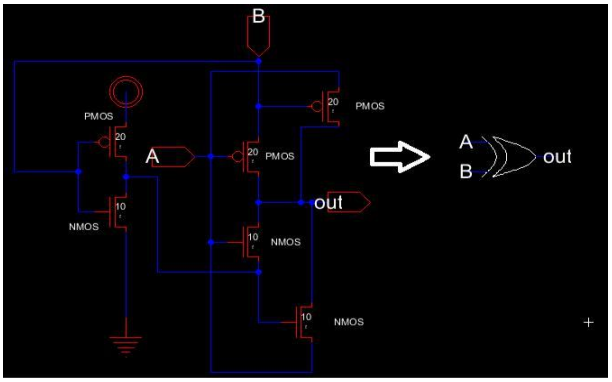

Fig 8: Schematic of Modified GDI XOR in Electric Software

AND gate is shown below

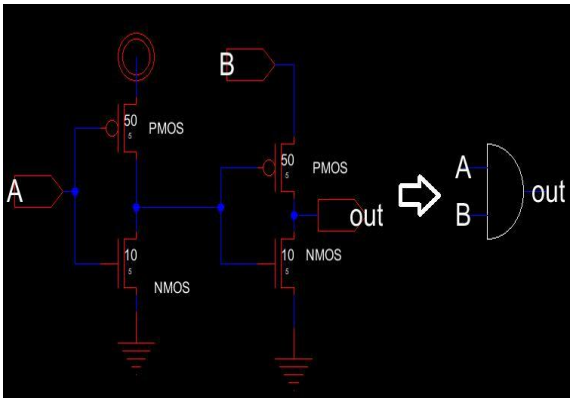

Fig 9: AND gate schematic

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OR gate is shown below

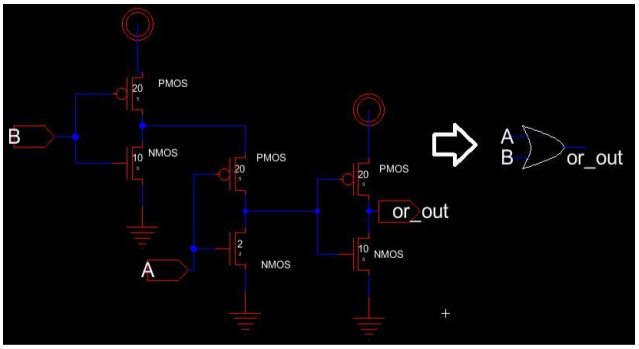

Fig 10: OR gate schematic

Basic Full Adder using two half adders is shown in the Fig 11

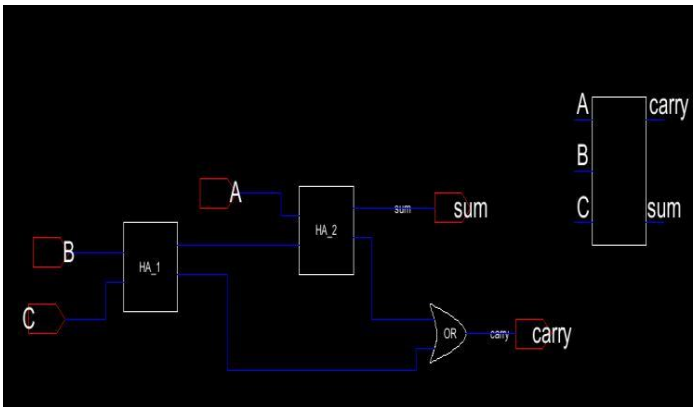

Fig 11: Full Adder using two half adders

4-bit RCA using FA is shown in the Fig 12.

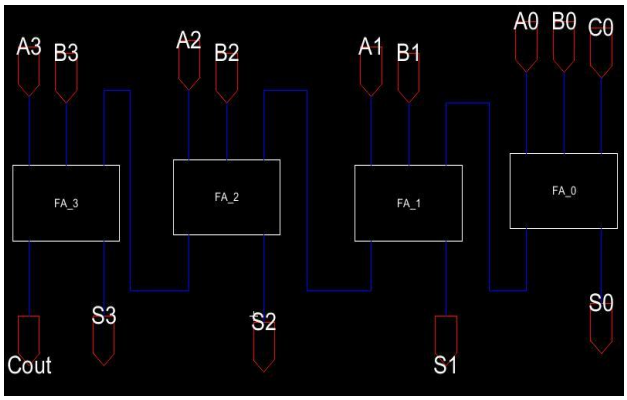

Fig 12: 4-bit Ripple Carry Adder

B. GDI BASED CLA

Carry Look Ahead adders are the fastest amongst all the other types of adders taxing on the hardware requirements. The ideal requirement is to obtain the fasters adder with optimum hardware and minimum power dissipation. The figure below shows the realisation of the 4-bit CLA using the Modified GDI cells mentioned in the section A.

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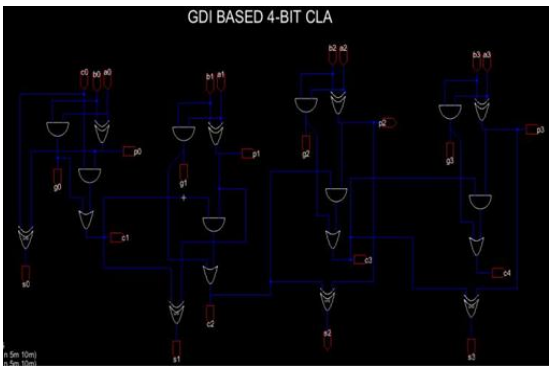

Fig 13: 4-bit Carry Look Ahead Adder

C. CARRY SKIP ADDER

The carry skip adders are faster than ripple carry adders; their speed of operation is comparable with CLA. Their area occupied on the silicon is less at the same time the total power dissipation is also less [4]. As the name suggests, in CSA the carry is skipped over a group of adder blocks, with the help of carry skip logic. Each adder works conventionally as to generate sum and carry. The carry skip logic is added to each of the adder block to detect as when the carry can be passed to the next adder block.Figure below shows the 4 bit carry skip adder

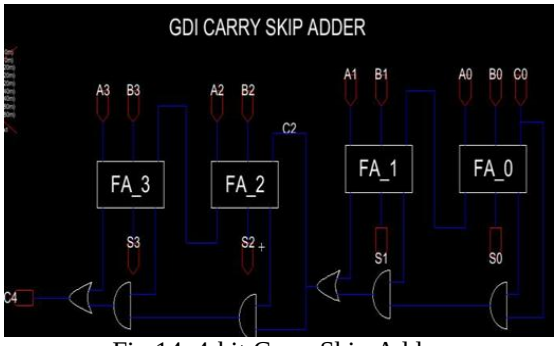

Fig 14: 4-bit Carry Skip Adder

Every FA block generates a block generator and a block propagate signal. The carry out of CSKA is written as

$C_{K+1}=G_K+P_KC_K$----------(5)

Here in CSKA the each block detects whether a carry is going to bypass the entire smaller Carry Propagation Block or not using the eq(5).

IV. SIMULATION RESULTS AND ANALYSIS

The schematic is drawn in with the help of Electric Software and the simulation is carried out in the LT-Spice software. Technology file of 130nm BSIM is used as the MOSFET model with V_{DD} of 1.2V.

The simulation result of modified GDI XOR cell is shown in the below Fig 15

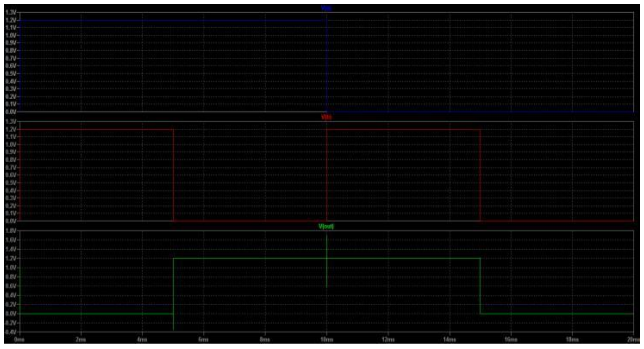

Fig 15: Waveform for XOR cell using Modified GDI cell

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Full adder is constructed using the modified GDI based cell and the waveform of that is shown in the figure below

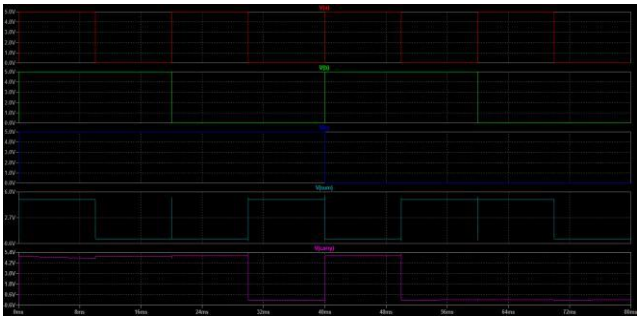

Fig 16: Waveform for FA using Modified GDI cell

Power Dissipation of M-GDI

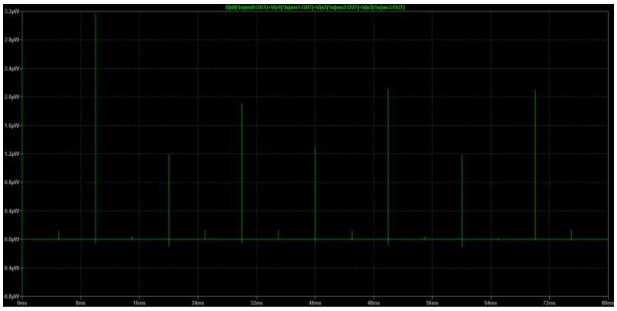

Fig 17: Average Power Dissipation in Modified GDI FA

The table 3 shows the transistor count, Power dissipation, delay and power delay product for the conventional COMS cells and modified GDI cell.

Table 3: Comparison of M-GDI adder with conventional CMOS

	Power Dissipation(fW)		Delay(ns)		Power Delay Product	
	CMOS	M-GDI	CMOS	M-GDI	CMOS	M-GDI
RCA	25.62	20.63	8.53	6.81	2.185 e-22	1.404 e-22
CSKA	30.41	28.52	3.39	2.89	1.031 e-22	0.879 e-22
CLA	236.3	128.4	3.32	3.11	7.847 e-22	7.35e -22

Looking at the table it is clear Modified GDI cell is performing better than CMOS variant in terms of all the testing parameter such as Average power dissipation, transistor count, propagation delay and Power Delay Product.

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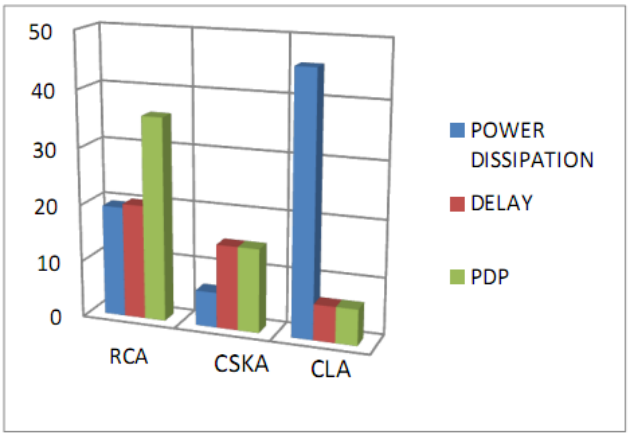

Fig 18: Comparison of RCA, CSKA, CLA for power dissipation delay and PDP

In above graph, it shows that CLA of M-GDI cell adder has 45% improvement in the average power dissipation compared to CMOS, RCA M-GDI call adder has 20% improvement in the delay and RCA M-GDI call adder has 35% improvement in the PDP.

V. CONCLUSION

In this paper a modified version of the GDI cell is proposed and tested. Though the traditional GDI is proved far superior in term of the performance of power consumption, propagation delay, transistor count and PDP, it suffers by the problem of logic degradation. So the modified GDI based circuits developed in this paperhas all the better qualities of GDI with the full logic swing. The M-GDI cell has consumed 45% less power as compared Conventional CMOS circuits, 20% reduction in the propagation delay and 35% less PDP. So the designed circuit can be used as t6he basic building block of the ALU unit as well as Digital Signal Processing applications, where speedy circuits which consume less power are the requirement.

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