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FPGA Implementation of Optimized Reversible Vedic Multiplier Architectures for High Speed Low Power Applications

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Abstract: Reversible logic is one of the most promising technology of the future computation, owing to its capability to tremendously reduce the dissipation of power. It has got extensive applications in emerging technologies such as quantum computing, optical computing, quantum dot cellular automata, ultra-low power VLSI circuits, advanced computing, DNA computing, Bio informatics and Nano technology. Since multipliers are one of the prominent building blocks of most of the computational units and since the speed of the computational units is largely determined by the speed of the multipliers, hence in order to increase the speed of computational units, we need to utilize faster multipliers. This is where Urdhva Tiryakbhayam (UT) Vedic multiplier comes into play. This multiplier performs the multiplication operation at a tremendously increased speed as compared to conventional multipliers, with decreased delay. This multiplier can be efficiently used in Digital signal processing system, Fast Fourier Transforms (FFTs), Filter design, Image processing and in other fast computational units including ALU. Thus we utilize the low power capability of reversible logic to reduce power dissipation and the high speed capability of Vedic multipliers to speed up the operation in our design. In this paper, we have shown the implementation of 4 different design architectures of Vedic multipliers using reversible logic which are optimized in terms of area, delay, power consumption and total computational complexity including quantum cost of the design. The design has been implemented on the Xilinx ISE Design Suite 14.7 using Verilog. The results of the analysis of all the 4 architectures with its computational complexity has been presented.

Keywords: Reversible logic, Garbage output, Quantum cost, Reversible multiplier, Vedic multiplier, Urdhva Tiryakbhayam Sutra, Reversible logic gates, UT Multiplier, Quantum computing.

I. INTRODUCTION

During the last decades, great achievements have been made in the development of computing machines. While computers consisting of a few thousands of components filled whole rooms in the early 70's, nowadays billions of transistors are built on some square millimetres. This is a result of the achievements made in the domain of semiconductors which are still holding on. The number of transistors in a circuit doubles every 18 months (which is also known as Moore's Law [9]. However, it is obvious that such an exponential growth reaches its limits, at least when the miniaturization reaches a level, where single transistor sizes are approaching the atomic scale. Besides that, power dissipation becomes a crucial issue for designing high performance digital circuits. During last decades, the amount of power dissipated in the form of heat to the surrounding environment of a chip has increased by orders of magnitudes. Since excessive heat may decrease the reliability of a chip (or even destroys it), power dissipation is one of the major barriers to progress the development of smaller and faster computer chips. [9]

Due to these reasons, some researchers expect that in the coming years, duplication of transistor density will not be possible any longer. To further satisfy the needs for more computational power, alternatives are needed that go beyond the scope of traditional technologies like CMOS. Reversible logic marks a promising new direction where all operations are performed in an invertible manner. That is, in contrast to traditional logic, all computations can be reverted (i.e. the inputs can be obtained from the outputs and vice versa [9].Reversible logic ensures zero information loss and low power dissipation. Groups like the Semiconductor Industries Association (SIA), in their annual study report called the International Technology Roadmap for Semiconductors (ITRS) predict that many areas where technological breakthroughs will be needed to ensure continued progress in the field computation. Reversible logic is one such breakthrough to carry the Moore's law into the future computing. This has motivated many research scholars and scientists to explore the area of reversible logic from various perspectives [25].

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II. LITERATURE SURVEY

Energy dissipation due to information losses in high technology system constructed using irreversible hardware was shown by R. Landauer [1] in 1960 where it is described that logical reversibility is associated with physical reversibility and requires a minimal heat generation per machine cycle and also states that logic computation that are not reversible necessarily generate $kT * \ln 2$ joules of heat energy for every bit of information that is lost, where $k = 1.3806505 \times 10^{-23}$ joules/kelvin is the Boltzmann's constant and T is the absolute temperature at which computation is performed. For room temperature this amount of heat dissipation can be small but not negligible. This amount may not seem to be significant but it will become relevant in the future.

In 1965, Gordon. E. Moore [2] forecast that a number of transistors on a chip would double every two years and so. His work is known as Moore's law. Due to the effect of Moore's law the number of components on chip will lead to increase in the power dissipation. The amount of power dissipated is equal to the heat dissipated in the chip. Therefore, power minimization has become an important factor. According to 'Moore's law', stated by Gordon Moore, Intel Co-founder, the performance of integrated circuits improve at an exponential rate with the performance per unit cost increasing by a factor of 2 every 18 months. This resulted in shrinking the dimensions on integrated structures to make it possible to operate at higher speed for the same power per unit area [2]. One should not forget that there is a minimum of quantum energy associated with elementary levels which puts a fundamental limit on the miniaturization. So the question is, is Moore's law going to end? Using current technology more and more components are getting packed onto the chip and at the same time the power dissipation in the present day computer is also not negligible. So, one of the major current research trends is towards saving of the power.

Further in 1973 C.H. Bennett [3] has stated that if a computation is carried out in reversible logic, zero energy dissipation is possible as the amount of energy dissipated in system is directly proportional to the number of bits erased during computation. The design that does not result in information loss is irreversible. A set of reversible gates are needed to design reversible circuits. He revealed that the computation which is performed on irreversible gates or model machines, can also be performed with same efficiency on the reversible gate. Edward Fredkin and Tommaso Toffoli in 1980's [4][5] have introduced new reversible gates known by their names as Fredkin & Toffoli gates which works on the principle of reversibility. These gates are universal gates with 3 inputs and 3 output terminals and hence also known as 3*3 reversible gates. These reversible gates have almost zero power dissipation. Later on, Peres [6] in 1985, acquainted a new gate which is known as Peres gate (3*3gate) but not a universal gate. It is widely used in most of the designs among all the gates due to its reduced quantum cost (4) as compared to the universal gates.

Rakshith saligram et.al. [13] in 2013, proposed two new architectures for the Vedic multiplier using BVPPG gate, which showed considerable improvements from the earlier design architectures of optimized multipliers. B.Ravali et.al.in 2015 [17], proposed a new architecture for the Vedic multiplier using BME gate with significant reduction in cost metrics including constant inputs, Quantum cost and overall TRLIC.

III. REVERSIBLE LOGIC

A Reversible Logic gate is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. This not only helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs. Because of this bijective mapping the output vectors are merely permutations of the input vectors.One of the advantages of reversible logic design is that it has theoretically zero internal power dissipation because it does not lose information. On the other hand, reversible logic design is an interesting and important area of study because it is very necessary in quantum computation. Quantum gates are introduced based on quantum computing theory. Quantum circuits are reversible because a closed quantum mechanical system is inherently reversible [26].

Reversible logic circuit implementations are also found in nanotechnology, low power CMOS design, optical information processing, quantum computing, thermodynamics, adiabatic CMOS, and DNA computing. A circuit is reversible if and only if the input vector can be uniquely recovered from the output vector. That is, there is a one-to-one mapping between its input and output vectors. Thus, a reversible logic circuit has equal number of inputs and outputs. Such circuits allow the reproduction of the inputs from observed outputs and we can determine the inputs from the outputs [26].

Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility. The benefits of logical reversibility can be gained only after employing physical reversibility. Physical reversibility is a process that dissipates no energy to heat. Absolutely perfect physical reversibility is practically unachievable [24]. Computing systems give off heat when voltage levels change from positive to negative: bits from zero to one. Most of the energy needed to

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make that change is given off in the form of heat. Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minute amount of energy on each transition. Reversible computing strongly affects digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs. It will impact instruction sets and high-level programming languages as well. Eventually, these will also have to be reversible to provide optimal efficiency. In the design of reversible logic circuits the following points must be considered to achieve an optimized circuit [24].They are

- Fan-out is not permitted.
- Loops or feedbacks are not permitted
- Garbage outputs must be minimum
- Minimum delay
- Less Constant/Ancilla inputs
- Minimum quantum cost [24].

A. Reversible Logic Gates

The basic reversible gates that has been used in the design are the following:

1) Feynman Gate [FG]: The Feynman gate (FG) or the Controlled-NOT gate (CNOT) is 2x2 reversible gate and has a quantum cost of 1. The block diagram and the quantum representation of Feynman gate is shown below.

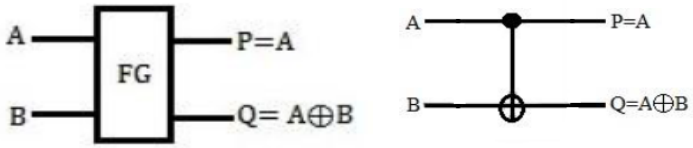

Fig 1: Block diagram and quantum representation of Feynman gate

2) Peres Gate [PG]: Peres gate is a 3x3 gate and it has a quantum cost of 4. The block diagram and the quantum representation of Peres gate is shown below.

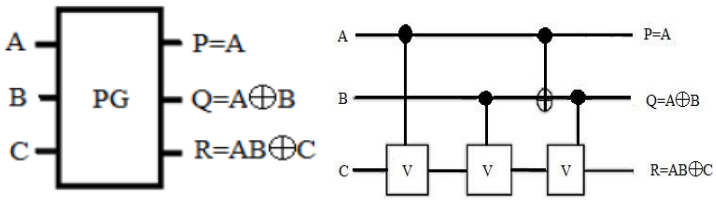

Fig 2: Block diagram and quantum representation of Peres gate

3) Toffoli gate (TG): It is a 3x3 gate with quantum cost of 5. The block diagram and the quantum representation of the same is shown below.

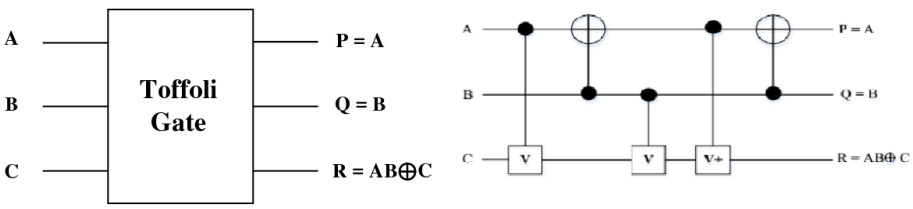

Fig 3: Block diagram and quantum representation of Toffoli gate

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4) New Fault Tolerant Gate (NFT gate): It is a 3*3 gate with the Quantum cost of 5. The block diagram and the quantum representation of the same is shown below.

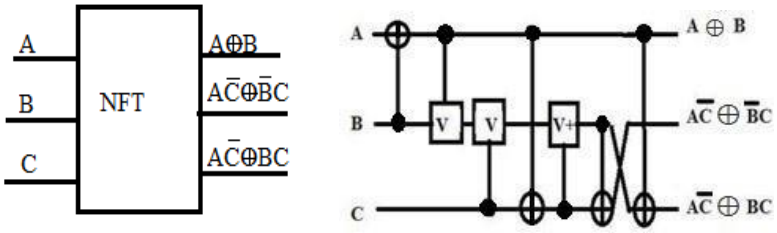

Fig 4: Block diagram and quantum representation of NFT gate

5) BME Gate: BME is a 4*4 reversible gate with the quantum cost of 5. The block diagram of the same is shown below.

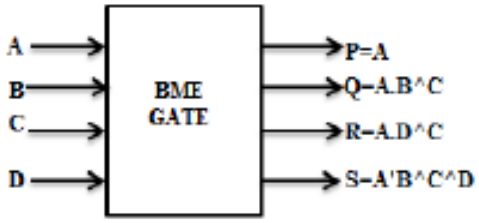

Fig 5: Block diagram of BME gate

6) HNG Gate: It is a 4x4 gate with a quantum cost of six. The block diagram and the quantum representation of the same is shown below.

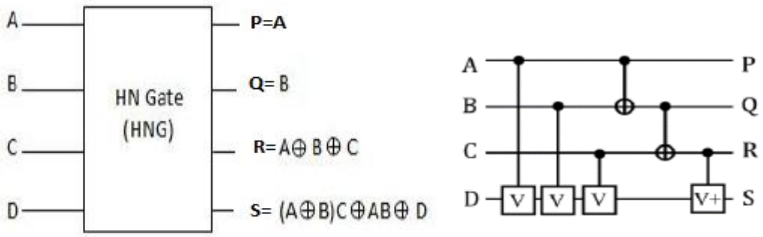

Fig 6: Block diagram and quantum representation of HNG gate

7) BVPPG gate: BVPPG gate is a 5 * 5 reversible gate. Its quantum cost is 10. The block diagram and the quantum representation of the same is shown below.

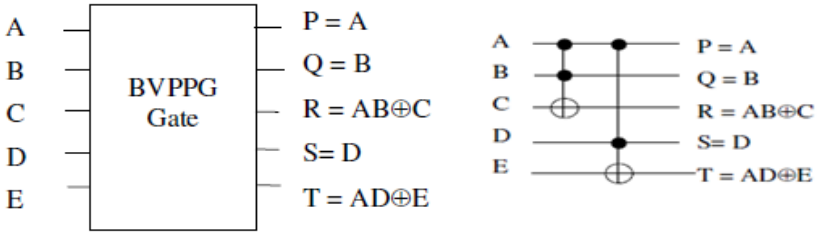

Fig 7: Block diagram and quantum representation of BVPPG gate

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B. Optimization parameters for reversible logic circuits

The important parameters which play a major role in the design of an optimized reversible logic circuit are as listed below:

- Constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- Garbage outputs (GO): This refers to the number of outputs which are not used in the synthesis of a given function.
- Gate count (NG): The number of reversible gates used to realize the function.
- Flexibility: This refers to the universality of a reversible logic gate in realizing more functions.
- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gates. It is calculated knowing the number of primitive reversible logic gates (1x1 or 2x2) required to realize the circuit
- Gate levels: This refers to the number of levels in the circuit which are required to realize the given logic functions.
- Total Reversible Logic Implementation Cost (TRLIC): Let, in a reversible logic circuit there are NG reversible logic gates, CI constant inputs, GO number of garbage outputs, and have a quantum cost QC. Then the TRLIC is given as TRLIC=NG+CI+GO+QC [9].

C. Applications of reversible gates

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance. It includes the areas like: Low power CMOS, Quantum computer, Nanotechnology, Optical computing, DNA computing, Computer graphics, Communication, Design of low power arithmetic and data path for digital signal processing (DSP), Field Programmable Gate Arrays (FPGAs) in CMOS technology [27].

The potential application areas of reversible computing include the following: Nano computing, Bio molecular Computations, Laptop/Handheld/Wearable Computers, Spacecraft ,Implanted Medical Devices ,Wallet “smart cards”, Smart tags on inventory.Prominent applications of reversible logic lies in quantum computers. Quantum gates perform an elementary unitary operation on one, two or more two–state quantum systems called qubits. Any unitary operation is reversible and hence quantum networks also. Quantum networks effecting elementary arithmetic operations cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible). Thus, Quantum computers must be built from reversible logical components [27].

IV.URDHVA TIRYAKBHAYAM SUTRA

Rapidly growing technology has raised demands for fast and efficient real time digital signal processing applications. Multiplication is one of the primary arithmetic operations every application demands. A large number of multiplier designs have been developed to enhance their speed. Active research over decades has led to the emergence of Vedic Multipliers as one of the fastest and low power multiplier over traditional array and booth multipliers. Vedic mathematics is an ancient system of mathematics based on 16 sutras. Since the mathematical operations using Vedic methods are quite fast, the computational speed to perform arithmetic operations in the processors can be improved .Vedic Multiplier deals with a total of sixteen sutras or algorithms for predominantly logical operations. A large number of them have been proposed using Urdhva Tiryakbhyam sutra rendering them most efficient in terms of speed [22].

The Vedic multiplication is based on an algorithm called Urdhva-Tiryakbhyam (vertical and crosswise) of ancient Indian Vedic mathematics. Urdhva-Tiryakbhyam Sutra: Consider two 2 bit binary numbers a_1a_0 and b_1b_0 as multiplicand and multiplier respectively. First, the least significant bits of the multiplicand and multiplier are multiplied vertically as shown in Fig.8 to give the lowest significant bit s_0 of the final product. Then, the product of a_0 bit of the multiplicand and b_1 bit of the multiplier is added to the product of b_0 bit of the multiplier and a_1 bit of the multiplicand (cross wise) as shown in Fig. 8 to give second bit s_1 of the final product and carry bit c_1. The most significant bit a_1 of the multiplicand and b_1 of the multiplier are multiplied vertically to obtain the third bit s_2 of the final product and the carry bit c_2 [22].

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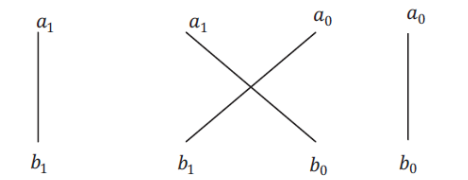

Fig 8: Urdhva-Tiryakbhyam Sutra

V.VEDIC MULTIPLIER IMPLEMENTATION

We have implemented 4 different architectures for the Vedic multiplier. All the 4 designs are implemented using both conventional RCA and the results are verified. The 4 design architectures are shown below.

*A. Design 1 for 2*2 UT Multiplier*

This design uses 5 Peres gates and one cnot gate. The design thus uses 6 gates, 4 constant inputs, 7 Garbage outputs and has a Quantum of 21.

*B .Design 2 for 2*2 UT Multiplier*

This design uses one BVPPG gate, 3 Peres gates and one Feynman gate. The design thus uses 5 gates, 5 constant inputs, 5 Garbage outputs and has a Quantum of 23.

*C. Design 3 for 2*2 UT Multiplier*

This design uses one BVPPG gate, 2 Peres gates and one NFT gate and one Feynman gate. The design thus uses 5 gates, 5 constant inputs, 4 Garbage outputs and has a Quantum of 24.

*D. Design 4 for 2*2 UT Multiplier*

This design uses one BME gate, 3 Peres gates and one Feynman gate. The design thus uses 5 gates, 4 constant inputs, 6 Garbage outputs and has a Quantum of 18.

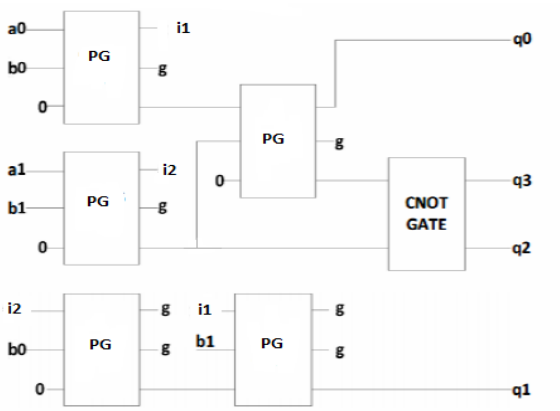

Fig 9: 2x2 UT Multiplier Design 1

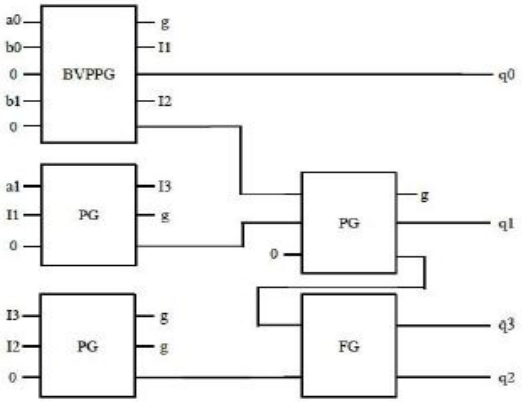

Fig 10: 2x2 UT Multiplier Design 2

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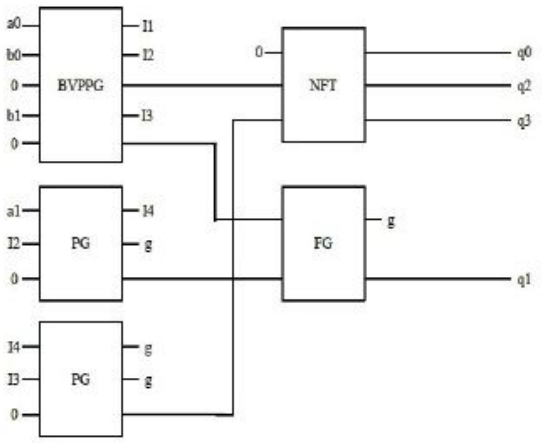

Fig 11: 2x2 UT Multiplier Design 3

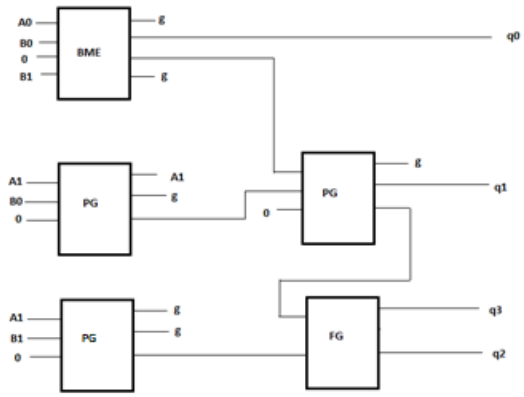

Fig 12: 2x2 UT Multiplier Design 4

The 4*4 multiplier using any of the four designs can be implemented as shown below. It makes use of four 2*2 UT multipliers, two 4 bit ripple carry adders ,a half adder and a 2 bit adder as shown below:

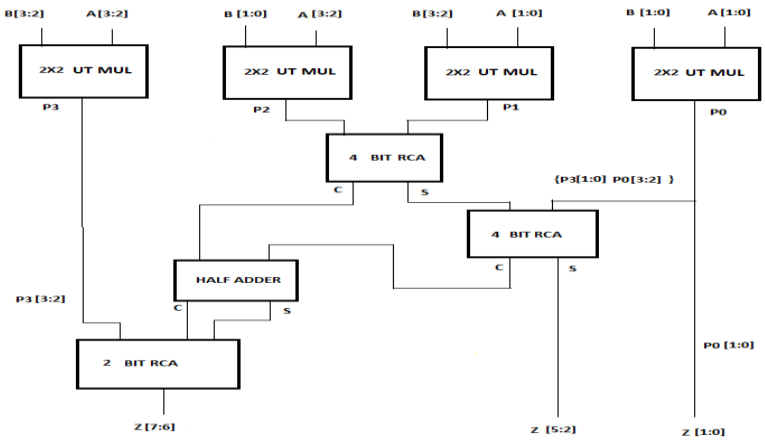

Fig 13: 4x4 UT multiplier

The 8*8 multiplier using any of the four designs can be implemented as shown below.. It makes use of four 4x4 UT multipliers, two 8 bit ripple carry adders, a half adder and a 4 bit adder as shown below.

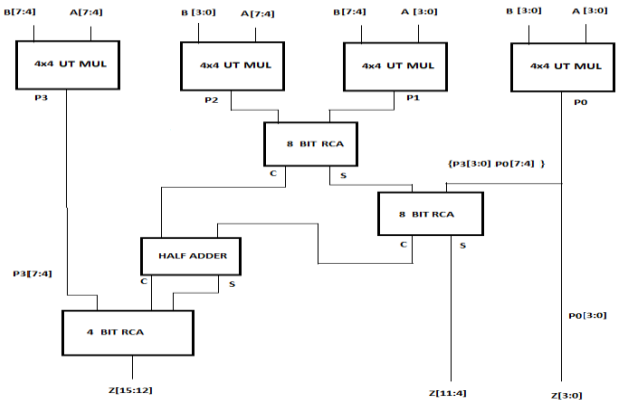

Fig 14: 8*8 UT Multiplier

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The implementation of 16*16 multiplier using any of the four designs can be done as shown below. It makes use of four 8*8 UT multipliers, two 16 bit ripple carry adders, a half adder and an 8 bit adder as shown below.

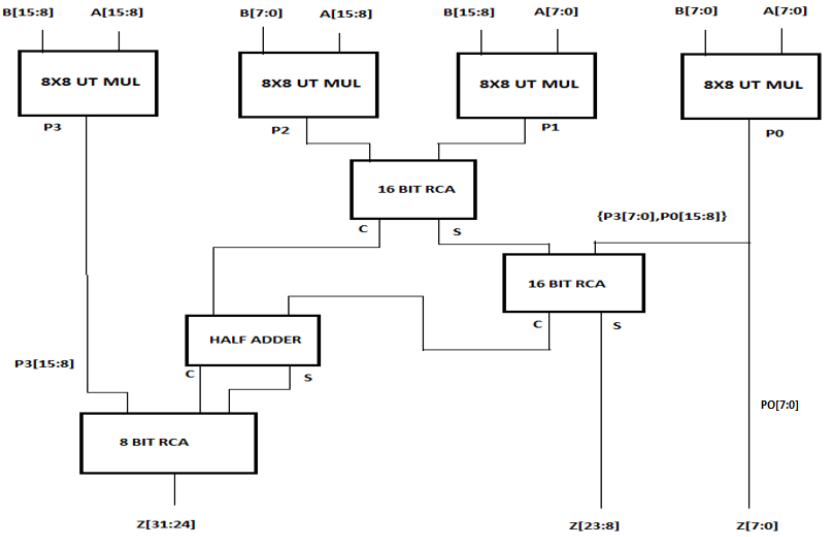

Fig 15: 16*16 UT Multiplier

VI. RESULTS AND COMPARISONS

In this paper, we have implemented 4 different design architectures of Vedic multipliers using reversible logic which are optimized in terms of area, delay, power consumption and total computational complexity including quantum cost of the design. The design has been implemented on the Xilinx ISE Design Suite 14.7, using Verilog. The results of the analysis of all the 4 architectures with its computational complexity has been presented. The block level diagrams of the units and results of simulation are shown below.

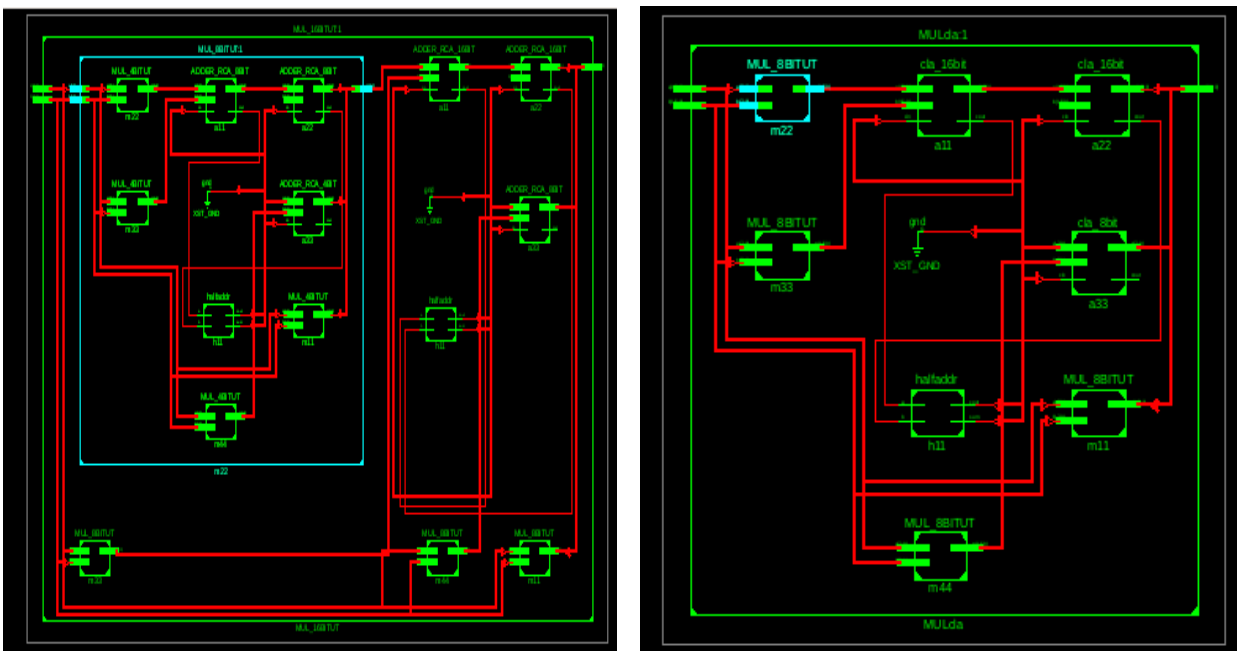

Fig 16: Block level representation of multipliers

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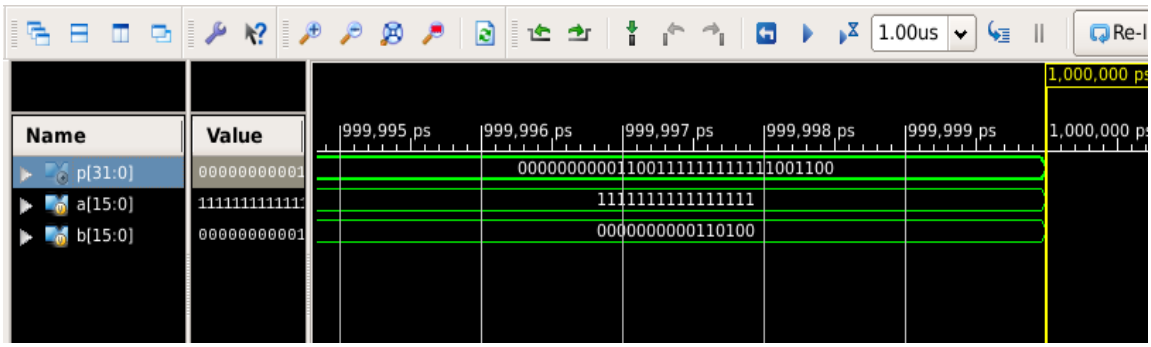

Fig 17: Simulation result of 16*16 multiplier in binary system

A. Analysis & comparison of various multiplier designs

Tables I, II & III show the comparison of all the four design architectures for 4*4, 8*8 and 16*16 multipliers respectively in terms of its cost metrics.

TABLE I: COST METRICS FOR 4*4 UT MULTIPLIER

4*4 Multiplier design	NG	CI	GO	QC	TRLIC
Design 1	35	27	46	142	250
Design 2	31	31	38	150	250
Design 3	31	31	34	154	250
Design 4	31	27	42	130	234

TABLE II: COST METRICS FOR 8*8 UT MULTIPLIER

8*8 Multiplier design	NG	CI	GO	QC	TRLIC
Design 1	161	129	222	686	1198
Design 2	145	145	190	718	1198
Design 3	145	145	174	734	1198
Design 4	145	129	206	638	1118

TABLE III: COST METRICS FOR 16*16 UT MULTIPLIER

16*16 Multiplier design	NG	CI	GO	QC	TRLIC
Design 1	685	557	966	2982	5190
Design 2	621	621	838	3110	5190
Design 3	621	621	774	3174	5190
Design 4	621	557	902	2790	4870

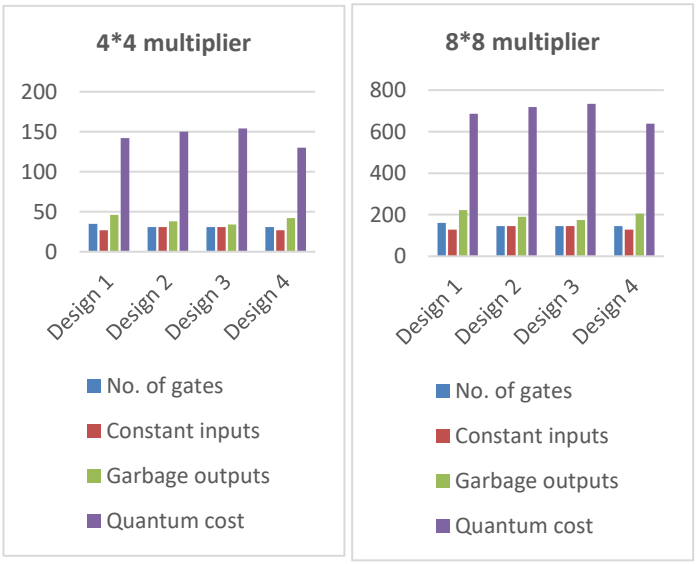

Fig 18: Comparison of the cost metrics for 4*4 and 8*8 multipliers

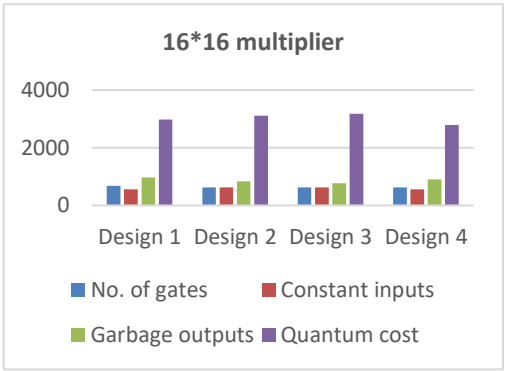

Fig 19: Comparison of the cost metrics for 16*16 multiplier

VII. CONCLUSION

It is a well-known fact that reversible logic gates are inevitable in a number of future computing technologies including quantum computing. In this paper we present four different design architectures for the Vedic multiplier. Of the four designs architectures design-4 is found to be more efficient compared to rest of the designs in terms of its cost metrics including quantum cost. Significant reduction in gate count, constant inputs, garbage output, Quantum cost and overall TRLlC is observed in the case of design 4 from the implementation. The paper can further be extended towards the process of digital design using reversible logic with applications in the fields of quantum computing, low power CMOS, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, image processing computer graphics etc.

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