IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Vol. 8, Issue 4, April 2021

DOI: 10.17148/IARJSET.2021.8443

NOVEL HYBRID MULTILEVEL SINGLE PHASE INVERTER

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Abstract: Multilevel inverters have created a new wave of interest in industry and research. While the classical topologies have proved to be a viable alternative in a wide range of high-power medium-voltage applications, there has been an active interest in the evolution of newer topologies. Reduction in overall part count as compared to the classical topologies has been an important objective in the recently introduced topologies. In this paper, some of the recently proposed multilevel inverter topologies with reduced power switch count are reviewed and analyzed. The paper will serve as an introduction and an update to these topologies, both in terms of the qualitative and quantitative parameters. Also, it takes into account the challenges which arise when an attempt is made to reduce the device count.

1.INTRODUCTION

Multilevel inverters (MLIs) are finding increased attention in industries as a choice of electronic power conversion for medium voltage and high-power applications. Multilevel inverter improves the output waveform and reduces its respective harmonic content, the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation. Multilevel inverters offer many benefits for higher power applications. In particular, these include ability to synthesis voltage waveforms with lower harmonic content than two level converters and operation at higher DC voltages using series connected semiconductor switches. The desired output from an inverter is a sinusoidal waveform which is a continuous function of time. However, use of power switches to implement a static inverter results in output waveform composed of discrete values. In other words, the waveform has fast transitions (dv/dt) rather than smooth ones. In order to imitate a sinusoidal waveform, two (or three) level inverters use pulse-width modulation (PWM) operation with high switching frequency, so that the fundamental component of the output is sinusoidal. This also eliminates the lower order harmonics. Apart from the issue of high switching losses due to high switching frequency, another issue that limits the feasibility of conventional two-level inverters for high-power high or medium–voltage applications is unavailability of high voltage/high power semiconductor switching devices.

Multilevel inverters are an attractive alternative to improve the output by synthesizing a staircase waveform imitating a sinusoidal waveform. Such a waveform not only has a low distortion, but it also reduces the dv/dt stress. Multilevel inverter topologies have the advantages of overcoming voltage limit capability of semiconductor switches, high voltage capability and better harmonic profile. Various multilevel inverter (MLI) structures are reported but the cascaded MLI (CMLI) appears to be superior to other inverter topologies in

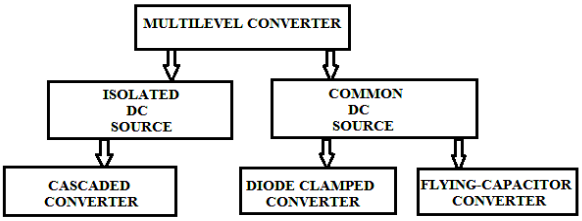

Fig2.1 Different Topology of Multilevel Inverter

application at high power rating due to its modular nature of modulation, control and protection requirements of each full bridge inverter (FBI). CMLI synthesizes a medium voltage output based on a series connection of power cells that use standard low-voltage component configurations. This characteristic allows one to achieve high-quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy.

Most of the modulation methods developed for MLI is based on multiple-carrier arrangements with pulse width modulation (PWM). The carriers can be arranged with vertical shifts (phase disposition, phase opposition disposition, and alternative phase opposition disposition (APOD) PWM), or with horizontal displacements (phase-shifted carrier ((PSC) PWM). Space-vector modulation (SVM) is also extended for the MLI operation, offers good harmonic performance[1].

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This paper recounts the development of a novel hybrid multilevel single phase inverter that has 8 power switches and 4 power diodes to produce 31-levels in the output voltage with incorporating all features listed above. The topology was applied to an induction motor and the performance of the inverter is studied using MATLAB/ SIMULINK. And the hardware prototype is developed for the verification of concept and the output results are clearly presented.

3. TYPES OF MULTILEVEL CIRCUITS

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The most attractive applications of this technology are in the medium- to high-voltage range (2-13 kV), and include motor drives, power distribution, power quality and power conditioning applications. There are different types of multi level circuits involved. The first topology introduced was the series H-bridge design. This was followed by the diode clamped converter, which utilized a bank of series capacitors. A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors. In this design, the semiconductors block the entire dc voltage, but share the load current. Several combinational designs have also emerged some involving cascading the fundamental topologies. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. The most actively developed of multilevel topologies are listed in figure2.1

4. OPERATIONAL OVERVIEW

The proposed topology comprises bye-pass diode technique and common H-Bridge configuration to form hybrid multilevel inverter shown in Fig 3.1. The bye-pass diode technique is used to produce only positive voltage steps. In this technique a special circuit is employed i.e the power switches and the DC source are connected in series and the diodes are connected in parallel. To increase the number of voltage levels in the output a source, switch and diode is added to the byepass diode technique topology.

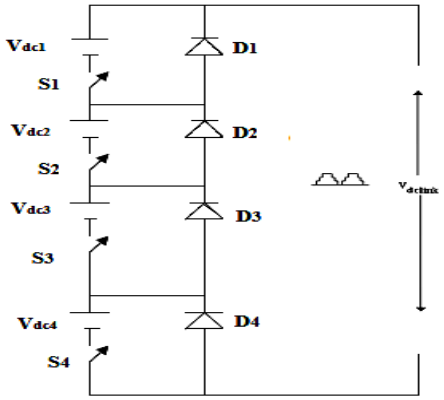

Fig 3.1 Byepass Diode Technique

The H-bridge circuit is used to produce both positive $(Q_{1,}Q_3)$ and negative (Q_2, Q_4) waveform in the output. The common H-bridge configuration is shown in the above fig 3.2. This H-bridge circuit remains constant for any number of levels produced by byepass diode technique. The switches $(Q_{1,}Q_3)$ will conduct during the positive half cycle and the switches(Q_2, Q_4) will conduct during the negative half cycle.

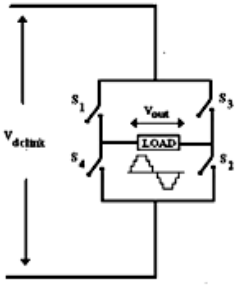

Fig 3.2 Common H-Bridge Configuration.

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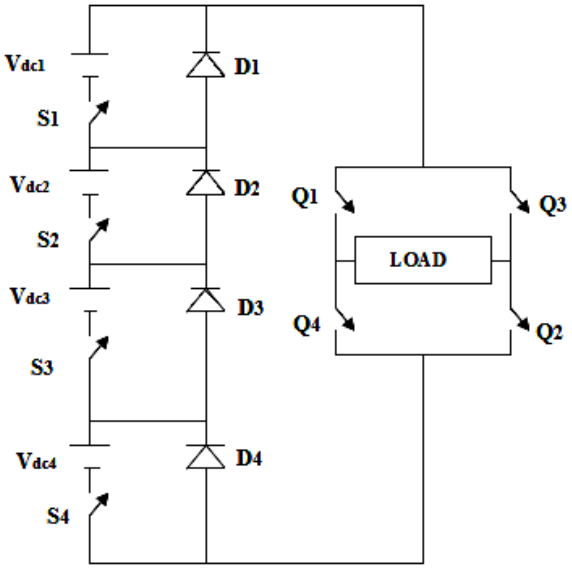

Fig 3.3

Proposed Circuit Diagram.

5. SIMULATION STUDIES

MATLAB is a high performance language for technical computing. It integrates computation, visualization and programming in an easy way to use in environment where problems and solutions are expressed in familiar mathematical notation. Typical uses include math and computation algorithm development, Data acquisition modeling simulation and prototyping data analysis exploration and visualization scientific and engineering graphics development including graphical user interface building. The MATLAB/SIMULINK toolbox is mainly used.

6. SIMULATION RESULTS

6.1 SIMULATION OF 31-LEVEL SINGLE PHASE INVERTER

The simulation circuit of the proposed inverter which comprises 10 IGBT switches and 4 diodes for producing 31-output voltage levels is shown in the figure 4.1

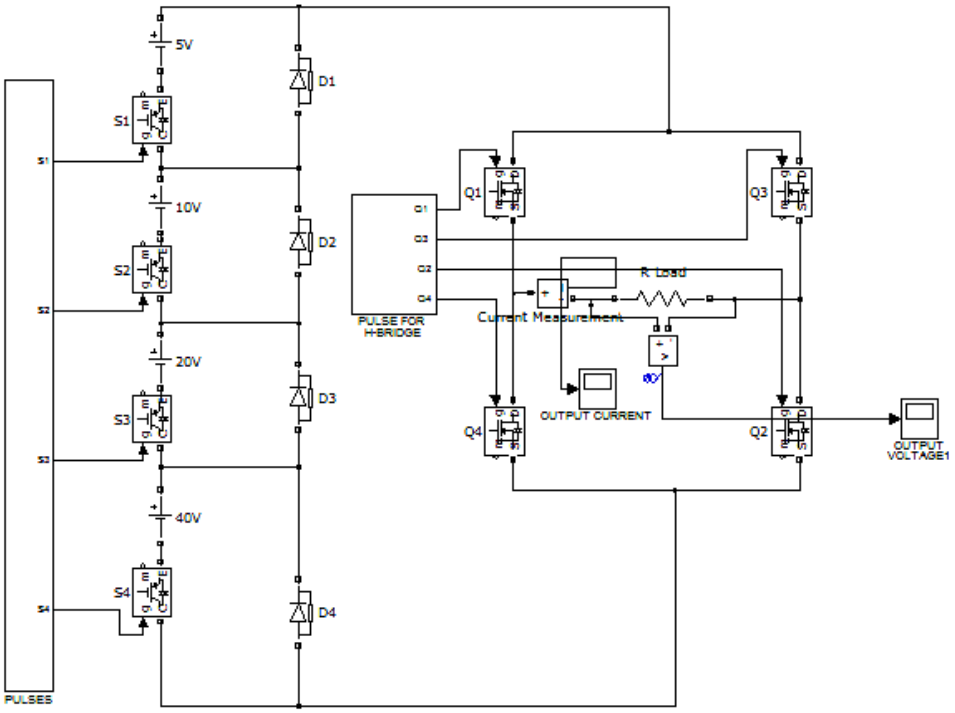

Fig 4.1 Simulink Model For single Phase system.

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6.2 SIMULATION OF 31-LEVEL THREE PHASE INVERTER

The induction motor is taken as load for inverter from the electrical machines block in the simpowersystem. Since the phase displacement blocks are connected to each output of the single phase inverter to produce the proper phase delay between the each phase it is shown in the fig4.3

To analyze various parameters like voltage waveform, current waveform, rotor speed and the electromagnetic torque of the induction motor scope is used. The output current waveform is used to analysis THD, which is select from powergui, then FFT analysis in which the signals are selected for the analysis and the THD will used to get displayed in FFT window.

The proper switching sequence (refer chapter 3 switching table 3.1) should be provided to the IGBT, the pulse generator is used to produce the reference pulse AND, NOT logic is used to produce the pulse for switches. For H-bridge inverter also AND, NOT logic is used. This method is simple and easy to adapt which are taken from the commonly used blocks.

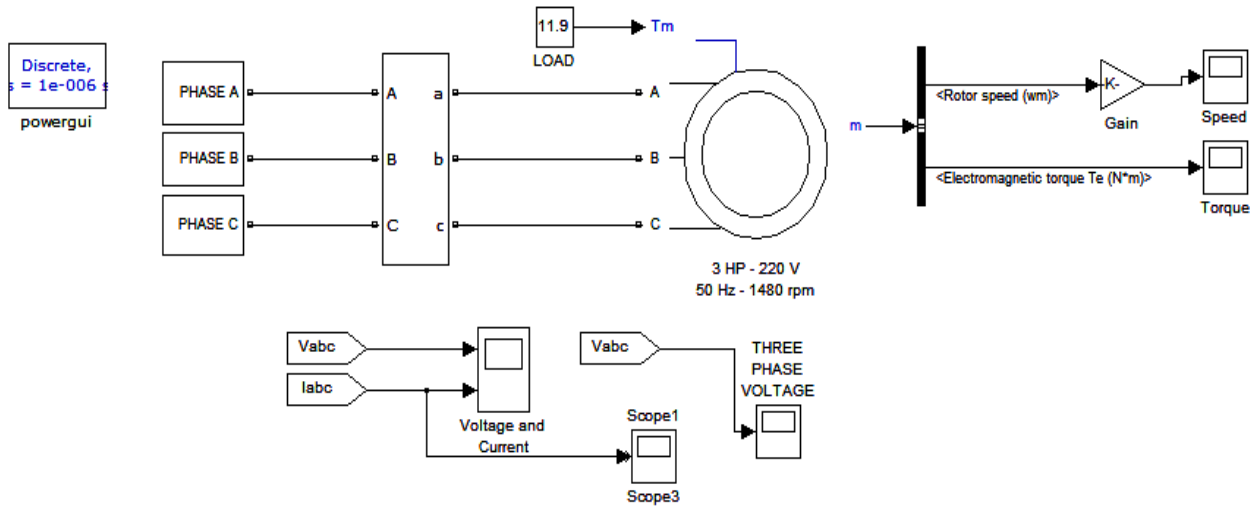

Fig4.3 Simulink Model for Three Phase.

6.3 SIMULATION RESULTS AND DISCUSSION

The computer simulation for the new topology of hybrid multilevel inverter has been done by using the MATLAB/SIMULINK. The output waveform has 31-levels in the positive side and 31-levels in the negative side and a zero level. This voltage levels are achieved with the help of four unequal voltage sources.
The positive and negative waveforms are produced with the help of H-bridge inverter.

The fig 4.3 shows the 31-level inverter output voltage waveform for peak voltage of 400V. Induction motor is connected as a load. The output waveform has 31-levels in both positive and negative half cycle that include zero level that occur twice in a cycle. It can be archived by connecting three separate single-phase and the phase delay is given with the help of phase delay block.

The Fig 4.5 shows the current waveform for three-phase inverter. From the curve we found that initially the current taken by the motor is high after a certain time it reaches the steady state. The current taken by the motor at steady state is 25A

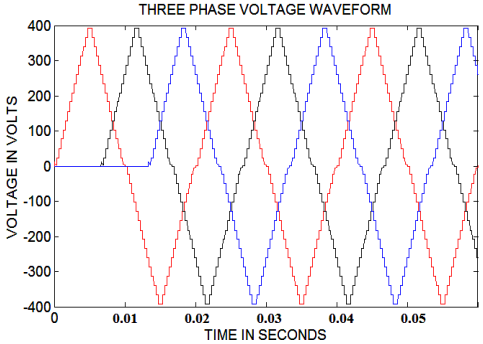

Fig 4.4 Three Phase Voltage Waveform

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The fig4.6 shows the electromagnetic torque of the induction motor. Initially the starting torque of the induction motor is very high up to 200Nm. Then in the steady state it reaches up to 20 Nm and maintain as a constant. Since the motor is connected to constant full load.

The comparison results are shown in following table 4.1

KEY FACTORS	SERIES PARALLEL SWITCHED MLI	DUAL BRIDGE MLI	PROPOSED HYBRID MLI
SWITCHING DEVICE	10	10	8
BYPASE DIODE	1		4
CLAMPING DIODE	-	-	-
DC SPLIT CAPACITOR	-	-	-
DC SOURCE	3	3	4
VOLTAGE LEVELS	15	15	31
THD	8.28%	8.18%	5.66%

TABLE 4.1 HARMONIC COMPARISON

8. CONCLUSIONS

Multilevel inverters offer improved output waveforms and lower THD. This project presents a new topology of hybrid multilevel inverter with reduced number of switches. A bypass diode technique is introduced to the conventional H-bridge multilevel inverter topology which reduces the number of controlled switches in the system. Only one H-bridge is required for the single phase system, plus a switch and a diode for each voltage source. Due to involvement of high number of switches in the conventional method the harmonics, switching losses, cost and the total harmonics distortion are increased. This proposed topology increases the output voltage level with less number of switches. It dramatically reduces the switches for high number of levels that in turn reduces the switching losses; cost and low order harmonics and thus effectively improves Total harmonics distortion reduction. To verify proposed hybrid multilevel inverter concept both simulation model and hardware prototype is developed and tested. Obtained from both the methods are analyzed. And the comparative study is made between hardware and simulation results a negligible deviation is observed between them.

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