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Fibonacci Series for Hybrid Symmetrical Multilevel Inverter Topology Using Different PWM Strategies

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Abstract:
Multilevel inverter attract with its high power and high voltage application. Multilevel inverters have uniq ue structure which makes it possible to reach high voltages with less harmonic content. In this paper, a Fibonacci seriesused for the value of DC source to obtain a new hybrid symmetrical topology multilevel inverter. The main advantage of proposed inverter has least Peak Inverse Voltage (PIV) than the other co nventional multilevel converter in both symmetric and asymmetric modes. Also, this topology doubles the number of output levels using only one cascaded four switches Hbridge cell.
This topology requires less number of components & less gate driver circuits as compared to conventional multilevel inverter topologies. This thesis has gives a brief summary of proposed MLI circuit topology (5-level and their analysis with different PWM techniques with the help of simulation by using MATLAB/SIMULINK.

Index Terms: Multilevel Inverter (MLI); Pulse width modulation (PWM) techniques, Peak Inverse Voltage (PIV) and Fibonacci series

1. INTRODUCTION:

The multilevel inverters are used in high power and high voltage industry. The main advantages of multil evel inverters are lower Total Harmonic Distortion (THD), less stress on the power switches and higher e fficiency. The harmonic content of the output decreases as the number of level increases. Multilevel invert ers enhances staircase waveform quality, it has less input current distortion, and lower electromagnetic inte rference. The multilevel inverters are used in drives, PV systems, and automotive applications. Three differ ent major multilevel converter structures have been useful in industrial applications: cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors.
The term multilevel began with the three-level converter are used to generate an AC voltage from DC voltage supply. The two-level inverter can only create two opposite polarity output voltages for the load, Vdc/2 or -Vdc/2. To build up an AC output voltage these two voltages are usually switched with PWM. To better underst and multilevel inverters the conventional three-level inverter, shown in Fig. 1. It is called a three-level inverter since every phase-leg can create the three voltage levels Vdc/2, 0, -Vdc/2

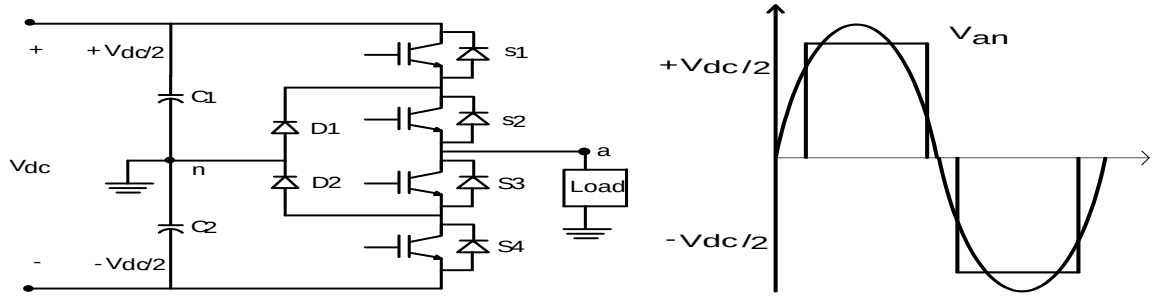

Fig .1: Circuit of single phase three-level inverter and three-level output voltage waveform.

The multilevel inverters are mainly classified as cascaded multilevel inverter, Diode clamped multilevel inv erter, flying capacitor inverter. The control method of cascaded H Bridge multilevel is more convenient th an other multilevel inverter because it doesn't have any clamping diode and flying capacitor. Cascaded m

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ultilevel inverter reaches higher reliability. The cascaded inverter is used for large automotive electric driv es.

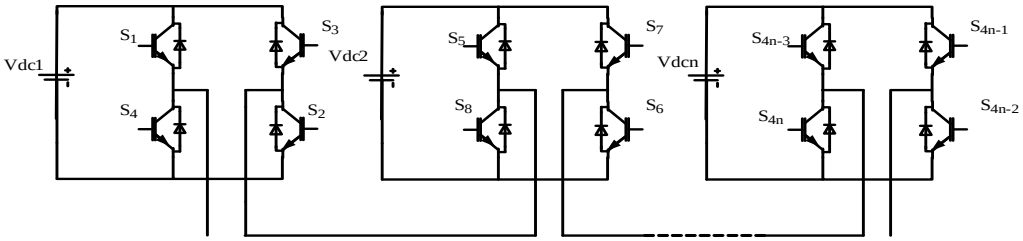

Fig. 2: Single phase cascaded multilevel inverter

One of the basic cascade H- Bridge multilevel inverter is show in fig.2. In cascade H-
bridge multilevel inverter each DC source is connected in different stages. If all DC source in Fig.2, equ al to V_{dc} = 1 Pu, then this converter is known as symmetric multilevel inverter. In symmetric topology, each unit generate three voltage levels $+V_{dc}$, 0, -
V_{dc}. The number of output voltage levels can be obtained by the equation: m = 2n + 1 and PIV is giv en by: PIV = $4nV_{dc,}$ Where n is the number of DC source and m is the number of voltage levels.

2. **Proposed Multilevel Inverter Topology:** conventional cascaded multilevel inverters require large nu mber
of switches and the power switches are combined to generate an output in positive and negative p olarities. In the proposed multilevel inverter there is no need to use all the switches in high frequ ency. In this new hybrid symmetrical topology different PWM scheme have been applied. In sym metrical mode the value of PIV and the number of switches versus other conventional symmetric converters has been reduced. For magnitude selection of DC voltage sources in asymmetrical mode Fibonacci series has been used. This cause significant reduction in total switches PIV with respect to other multilevel topologies.

   To increase the output voltage levels only four switches
   H- Bridge inverter are mixed by specific topology show in fig. 3 as series

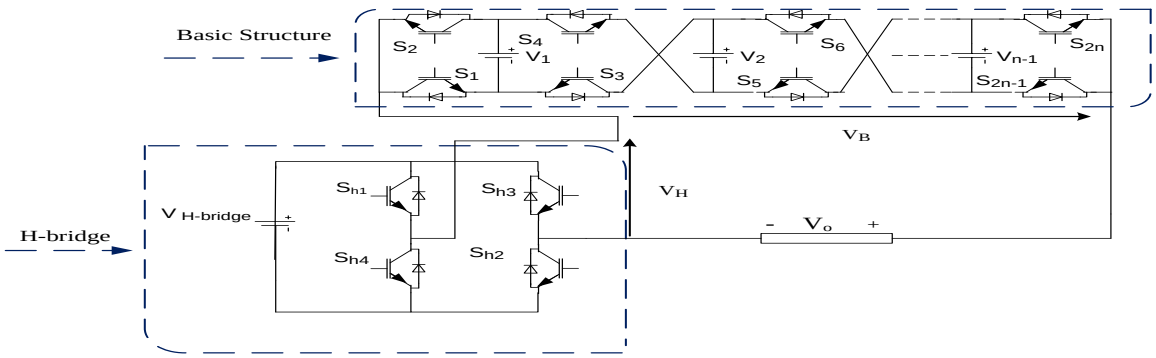

Fig.3: Proposed Structure

The proposed converter are show in Fig.3, with nDC source, in order to double the number of output voltage levels in specific configuration basic structure, H-
Bridge DC source is selected half of the minimum value of basic structure DC voltage sources. For exa mple, if all DC voltage sources in Fig. 3.3 are equal to Vdc = =1 Pu, selected value for H-

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Bridge DC source will be $1/2V_{dc}$ = 0.5pu. . In Fig. 3 value of $V_{H\text{-}bridge}$ is $V_{i\ (min)}=V_1/2$.Since in hybrid symmetric topology.The number of output voltage levels, is obtained by: m =4n - 1, where n is the number of DC voltage sources. The PIV value of hybrid symmetric topology is given by PIV= (4n-2) Vdc .

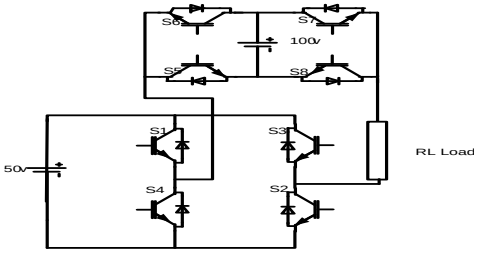
Modes of Operation

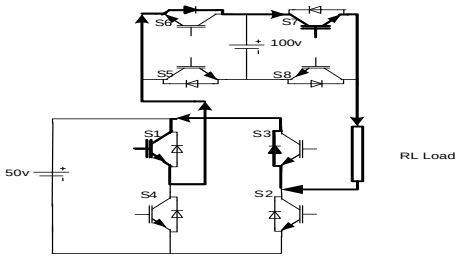
The Modes of Operation of suggested MLI is explained by Fig.4, (a), (b), (c), (d) and (e) depicts the arrangement of a 5-level Proposed MLI. The number of carrier signals is obtained by nCarrier = m - 1= 4 [27]. Fig.5 shows the output voltage of Vo. The output voltage frequency band is given in 5.25. The magnitude of each voltage source in basic structure is considered V=100 V and the value of voltage source in H-bridge cell is $V_{H\text{-}bridge}$=50 V. Table-1 shows ON state switches lookup table for each output voltage level

Table -1

VOLTAGE LEVEL	SWITCHING STATE								OUTPUT VOLTAGE
	S1	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*	
2	1	0	1	0	1	0	1	0	100
1	1	1	0	0	0	1	1	0	50
0	1	0	1	0	0	1	1	0	0
-1	0	0	1	1	1	0	0	1	-50
-2	0	1	0	1	0	1	0	1	-100

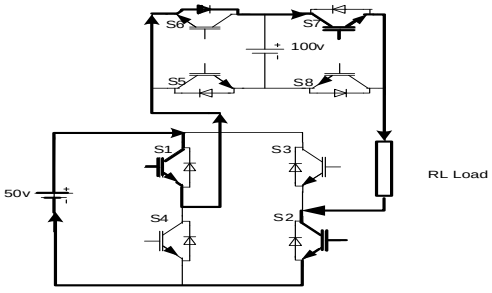
Mode of Operation suggests 5level MLI with single phase symmetrical Fibonacci topology can be easily explained with the help of fig.4. When switches S1, S3, S5 and S7 are turned “ON” the output voltage will be “100” (i.e. level five).The output voltage will be “50” (i.e. level four) when switches S1, S2, S6 and S7 are turned “ON”. When switches S1, S3, S6 and S7 are turned “ON” the output voltage will be “0” (i.e. level three). In level two Switches S3, S4, S5 and S8 are turned “ON” the output voltage will be “-50”. In level one switches S2, S4, S6 and S8 are turned “ON” the output voltage will be “-100”. And similarly for 7-level & 9-level of multilevel inverter.

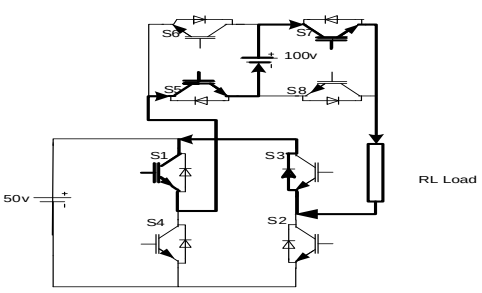




The configuration of a 5-level proposed Symmetric MLI (a)

(b)





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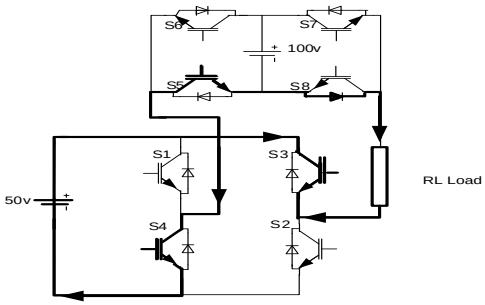
(d)



(e)

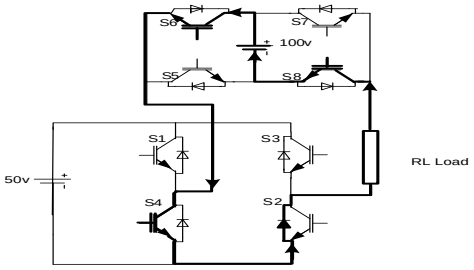


Fig.4 (a), (b), (c), (d) and (e) are switching combination of 5-level Fibonacci MLI

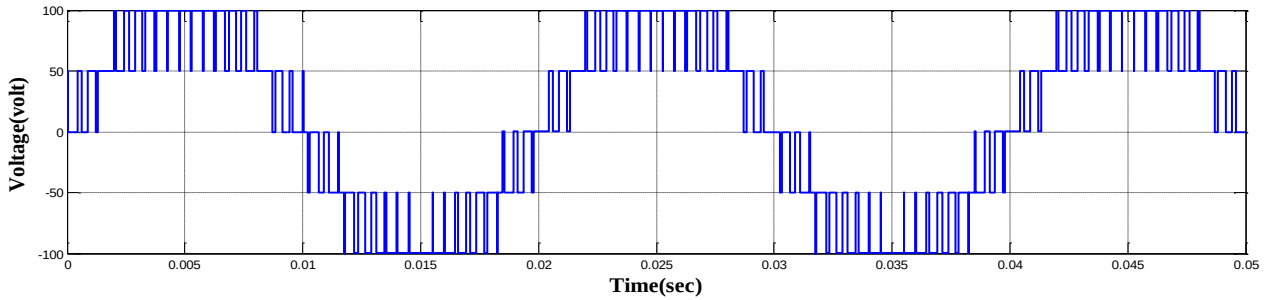


Fig.5 Output voltage for new topology of 5-level MLI

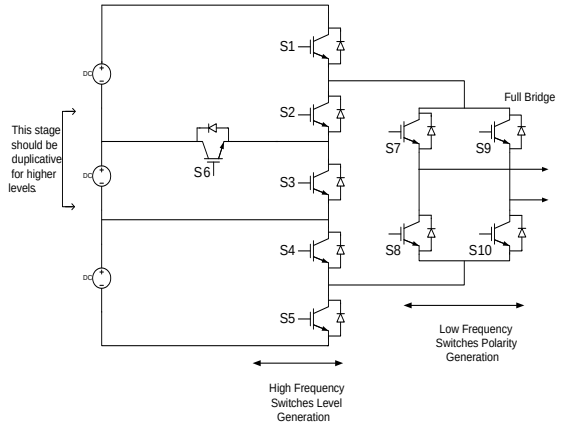


Fig.6 Proposed single-phase 7-level MLI topology

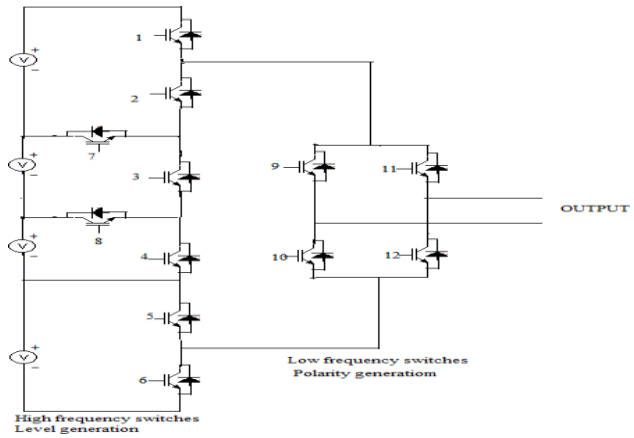


Fig.8 Proposed single-phase 9-level MLI topology

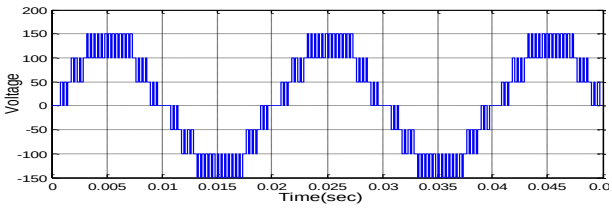


Fig.7 Output Phase Voltage of a 7-level MLI

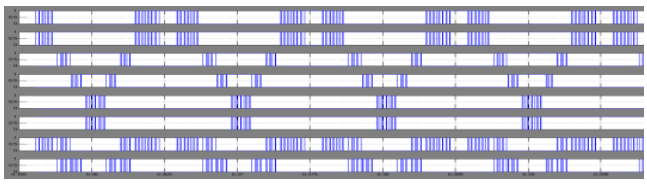


Fig.9 Output phase Voltage of a 9-level MLI

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3. MODULATION TECHNIQUE

In multilevel inverter there are different type modulation techniques can be applied. Every modulation tech nique has its own advantages and disadvantages depending on modulation index

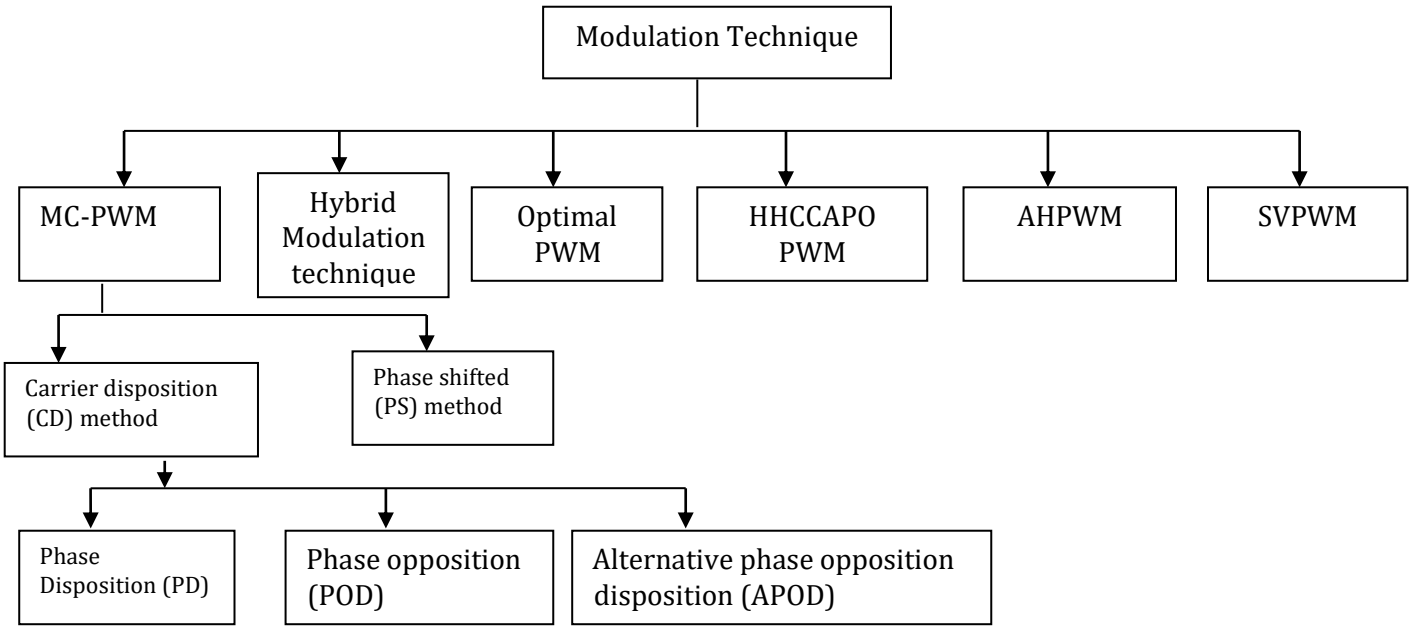

Fig.10 Block diagram for novel modulation techniques

Phase Disposition pulse width modulation (PD-PWM):-
In phase disposition pulse width modulation strategy, where all carrier waveforms are in phase with frequency andamplitude shown in fig.11 for 11-level MLI.
11 triangle carriers are required. For this technique, significant harmonic is concentrated at the carrier frequency.

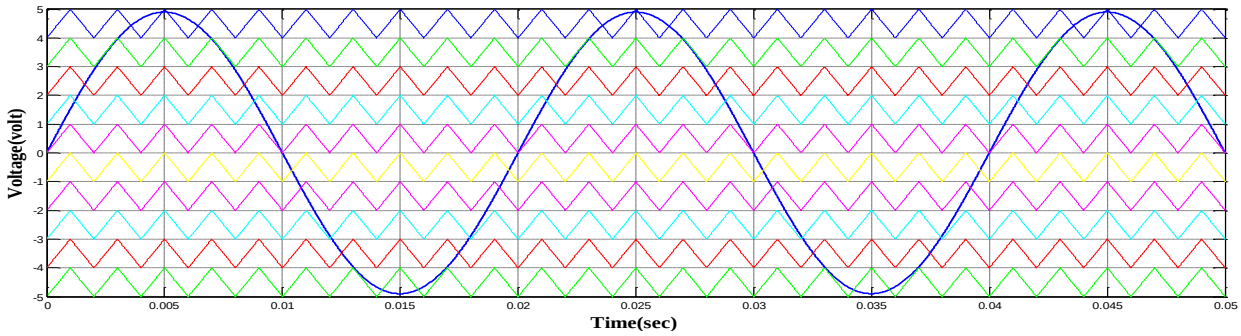

Fig. 11 Carrier arrangement for PDPWM strategy

Phase opposition disposition Pulse width modulation(POD PWM): In POD PWM strategy, where all car rier waveform are in phase to above zero reference and are 180^0 out of phase to below zero reference. In this modulation
technique, dominant harmonics are on the sideband of the first carrier ($m_f \pm 1$) and the phase voltage har monic at the carrier is not considerable.

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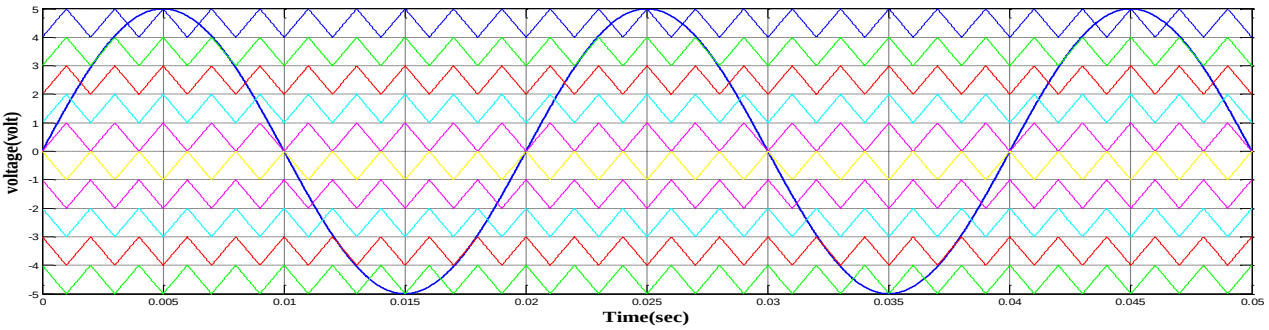


Fig.13: Carrier arrangement for PODPWM strategy

Alternate phase opposition disposition pulse width modulation (APOD PWM): In APOD PWM scheme where every carrier waveform is in out of phase with is neighbour carrier by 180^0. The APOD modulat ion technique does not produce a first carrier harmonic. Instead dominant harmonics are channelled into t he sideband around the first carrier harmonic. Therefore, since only the triple sidebands away from the ca rrier frequency cancel in the three phase system, APOD modulation contain some considerable harmonic e nergy in the line m_f is even. If m_f is odd, then the output waveform has odd symmetry.

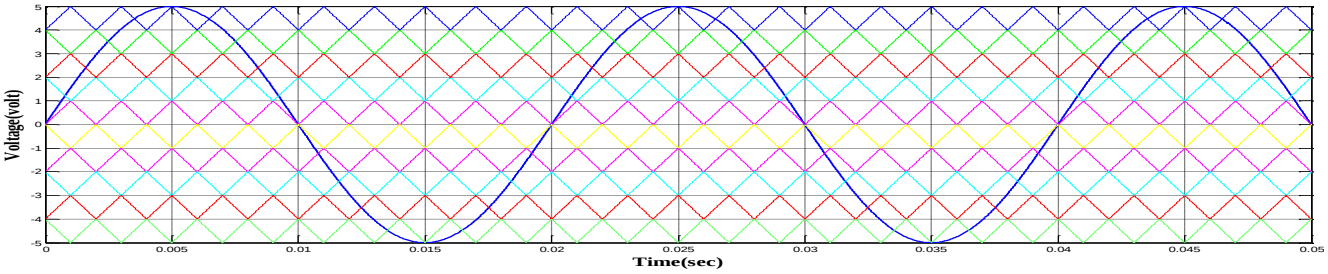
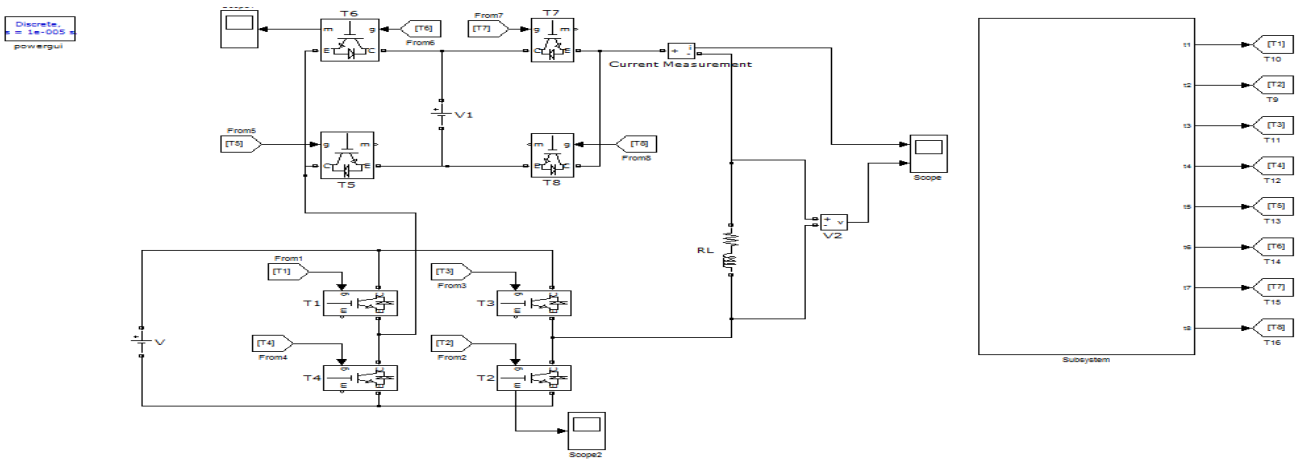


Fig.14: Carrier arrangement for APODPWM strategy

4. SIMULATION: Fig.5 shows the output voltage of a 5-level MLI. Table-3 represents THD at different modulation index. It can be observed that there are very few notches in the voltage and current waveforms. For 5-level MLI, corresponding (%) THD PD = 30.45, POD = 29.93, APOD = 30.24, ISC-PWM = 32.21 and VFIS = 32.14 at modulation index (Ma) = 0.9 and Mf = 20 are shown in Fig. 17-19 Comparative analysis of THD for different PWM techniques is given in Table-2

Fig.15 simulation model of a 5-level



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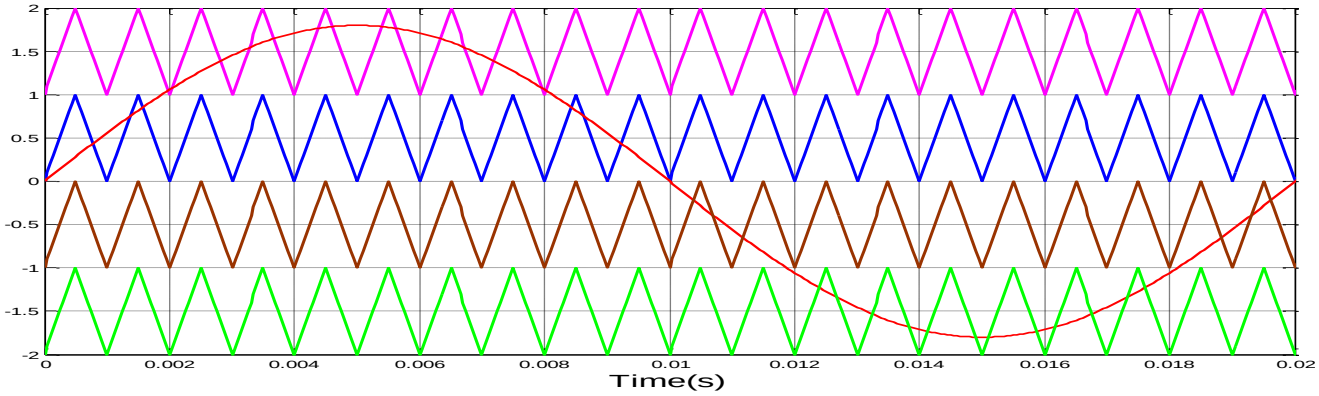

Fig.16 Carrier Modulation signals of single phase 5-level MLIF

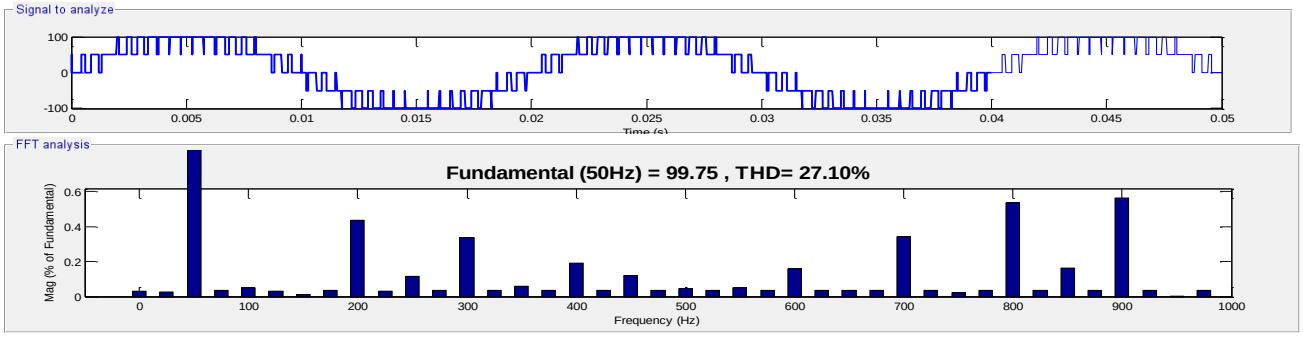

Fig.17 FFT Analysis for PDPWM with R-L Lo

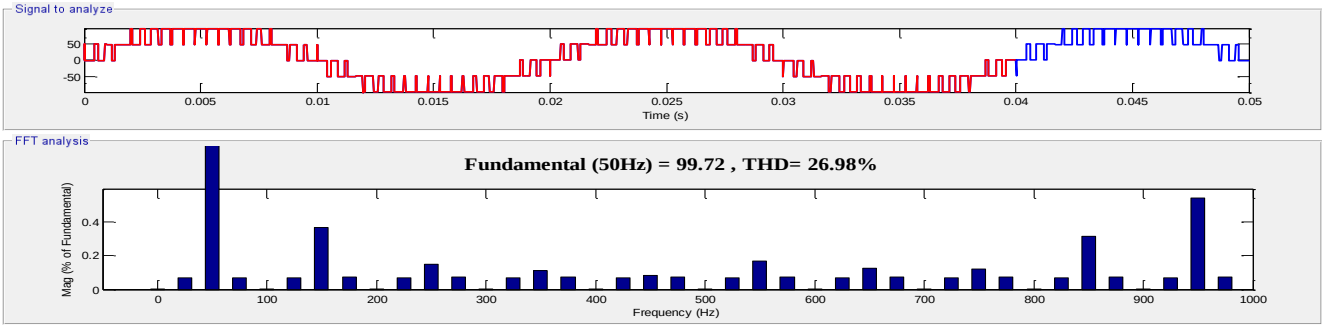

Fig.18 FFT Analysis for PODPWM with R-L Load

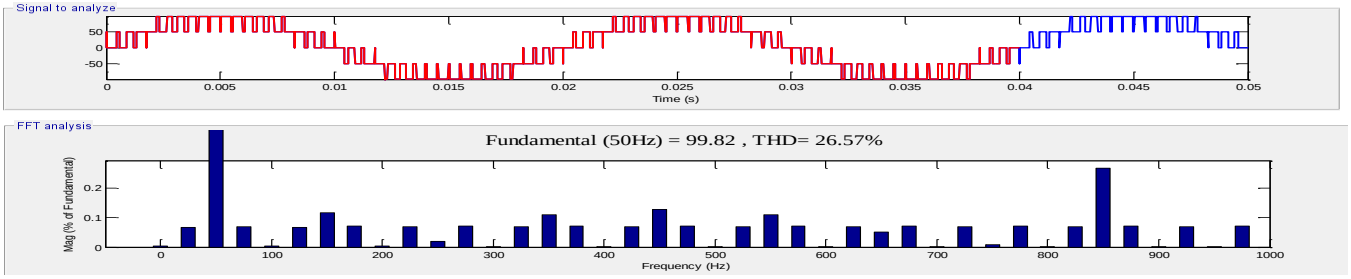

Fig.19 FFT Analysis APODPWM with R-L Load

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Table-2

PWM Technique	Modulation Index		
	0.8	**0.9**	**1**
PD-PWM %THD	33.69	30.45	27.10
POD-PWM %THD	33.55	29.93	26.98
APOD-PWM %THD	33.26	30.24	26.57

5. Conclusion: This thesis has gives a brief summary of proposed MLI circuit topology (5-level) and their analysis with different PWM techniques**.** In this thesis, a proposed Symmetric MLI topology the main feature is less PIV, required less number of switches compare to other conven tional MLI. And also is add some other benefit like less control requirements, cost, and reliability. This topology is used in power application such as FACTS, HVDC, and PV systems. In symmet rical hybrid proposed topology, PIV of switches is given by PIV = $(4n - 2)V_{dc}$. Table-3, summarizes the number of switches and PIVs for the symmetric cascaded multilevel inverter an d symmetric topology of and also proposed symmetric topology respectively, where n is the numb er of DC voltage sources. For generate same output levels number, the number of switches for sy mmetric proposed topology is fewer than other topologies. Also, with the same number of output voltage levels, a switch PIV for symmetric proposed topology is fewer.

Table-3

Symmetric Inverter	CMI	Semi cascade	Proposed
m (number of levels)	2n + 1	2n + 1	4n -1
PIV	$4nV_{dc}$	$(6n - 2)V_{dc}$	$(4n -2)V_{dc}$
Switches(IGBT)	4n	2n + 2	2n + 4

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