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Literature review on "Area-Delay-Power Efficient Carry-Select Adder"

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Abstract: In this paper, we made an analysis on the logic operations involved in conventional carry select adder (CSLA) and CSLA based on binary to excess-1 converter (CSLA-BEC) to study the data-dependency, and to find redundant logic operations. We have eliminated all the redundant logic operations of conventional CSLA, and proposed a logic formulation for CSLA. In the proposed scheme, the carry-select operation is scheduled before the calculation of final-sum, which is different from the conventional approach. A CSLA based on the proposed scheme generate n-bit carry-words corresponding to input-carry '0' and '1', where n is the input bit-width. These carry words follow a specific bit-pattern which can be used for logic optimization of carry-select unit. Fixed input bits of carry generator unit also can be used for logic optimization. Based on this, an optimized design for carry-select unit and carry generator unit are obtained. Using these optimized logic units, an efficient design is obtained for CSLA. Due to small carry-output delay, the proposed CSLA design is a good candidate for SQRT adder.

Keywords: Adder, BEC, Low power design, CSLA

I. INTRODUCTION

High-speed data path logic systems are one of the most substantial areas of research in VLSI system design. High performance, low power and area-efficient systems are increasingly used in portable devices. A complex digital signal processing (DSP) system involves several adders. An adder is the main component of an arithmetic unit. Adders are also used in multipliers, in high speed integrated circuits and in digital signal processing to execute various algorithms like FFT, IIR and FIR. On the basis of requirements such as area, delay and power consumption some of the complex adders are Ripple Carry Adder, Carry look-Ahead Adder and Carry Select Adder. Ripple Carry Adder (RCA) shows the compact design but their computation time is longer. Time critical applications make use of Carry Look-Ahead Adder (CLA) to derive fast results but it leads to increase in area. But the carry select adder provides a compromise between the small areas but longer delay of RCA and large area with small delay of Carry Look Ahead adder. A ripple carry adder uses a simple design, but carry propagation delay (CPD) is the main concern in this adder. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.

II. LITERATURE SURVEY:

[1] Carry Select Adder Using Common Boolean Logic

In Proposed Sqrt CSLA using Common Boolean Logic to remove the duplicate adder cells in the conventional CSLA, an area efficient SQRT CSLA is proposed by sharing Common Boolean Logic (CBL) term. While analyzing single bit full adder, results show that the output of summation signal as carry-in signal is logic "0" is inverse signal of itself as carry-in signal is logic "1". To share the Common Boolean Logic term, we only need to implement a XOR gate and one INV gate to generate the summation pair. And to generate the carry pair, we need to implement one OR gate and one AND gate. In this way, the summation and carry circuits can be kept parallel. This method replaces the Binary to Excess-1 converter add one circuit by common Boolean logic. As compared with modified SQRT CSLA, the proposed structure is little bit faster. In the proposed SQRT CSLA, the transistor count is trade-off with the speed in order to achieve lower power delay product. This work has been designed for 8-bit, 16-bit and 64-bit word size and results are evaluated for parameters like area, delay and power. It cannot be used for higher number of bits.

[2] Carry select adder using BEC and RCA

The Carry select adder (CSLA) is used in many computational systems to alleviate the problem of carry propagation

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delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input, then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA to achieve high speed and low power. In this paper, qualitative evaluations of the CSLA adder with and without BEC architectures are given. Among the huge member of the adders they wrote VERILOG (Hardware Description Language) code for Carry skip and carry select adders to emphasize the common performance properties belong to their classes. With respect to delay time and power consumption this paper concludes that the implementation of CSLA with BEC is efficient. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure consumption.

[3] An area-efficient carry select adder design by sharing the common Boolean logic term

An area-efficient carry select adder is proposed by sharing the common Boolean logic term. After logic simplification and sharing partial circuit, one XOR gate and one inverter gate in each summation operation as well as one AND gate and one inverter gate in each carry-out operation is needed. Through the multiplexer, correct output result is selected according to the logic state of carry-in signal. In this way, the transistor count in a 32-bit carry select adder can be greatly reduced. Moreover, the power consumption can be reduced as well as power delay product reduced.

[4] Lower Power High Performance Carry Select Adder

This work uses a sophisticated and efficient gate-level modification to significantly reduce the delay and power of the carry select adder and observing the structure of the CSA, it is clear that there is scope for reducing the delay and power consumption in the CSA. Based on this modification 8-, 16-, 32-, and 64-bit CSA architecture have been developed and compared with the regular CSA architecture. The proposed design has reduced delay as compared with the regular CSA with only a slight increase in area. This work evaluates the performance of the proposed designs in terms of delay, area, power, and their products by hand with using tools like synopsis (VCS), Xilinx ISE. The results analysis shows that the proposed CSA structure is better than the regular CSA according to delay.

[5] An Efficient 64-Bit Carry Select Adder With Less Delay And Reduced Area Application

In this paper an efficient approach is used to reduce the area and delay of SQRT CSLA architecture. The reduction in the number of gates is obtained by simply replacing the RCA with BEC in the structure. The compared results shows that the modified SQRT CSLA has a slightly larger area for lower order bits which further reduces for higher order bits. The delay is reduced to a great extent with the modified SQRT CSLA. This results shows that using modified method the area and delay will decrease thus leads to good alternative for adder implementation for many processors.
This approach is suitable only for lower order bits, it is not possible for higher order bits like 128,256 and more.

[6] Design of carry select adder based on a compact carry look ahead unit using 18nm FinFet technology

The approach is to construct a static and compact carry select adder using a conventional CSLA design. The Finfet technology is used in this paper and is much advanced with sophisticated specifications. The transistors that are present in finfet technology are used in place of Pmos and Nmos. They have faster switching rate than compared to Cmos technology. The produced noise margin is reduced with the help of a restoring inverter. The XOR gates which are used are made up of two level restoring circuits. Its drive current is extremely enormous in contrast with spillage current that implies proportion of on to it off current is exceptionally huge, and it is applicable only to speed up the devices with different specifications.

[7] Design and implementation of high speed carry select adder

A reduced power carry select adder is proposed which is implementing the clsa in arithmetic and logic unit (ALU), the john von Neumann proposed the ALU concept. The gates used in the proposed csla are, the AND and EX-OR are used as half sum generator. The OR and AND gate are used as carry generator and also in carry selector. Then EX-OR is used as full sum generator. The proposed CSLA has good amouny of reduction in terms of power and gate count. The reduced number of gates offers a advantage in the reduction of area and delay. The proposed csla has positive results as and when compared the BEC based and CBL based csla.

[8] Design of low power and efficient carry select adder using 3-T XOR gate

In the paper it proposes to build an efficient carry select adder using 3-t XOR gate, which has a large decrease in switching transistors. A single modified xor gate used in this work has 9 less transistors as compared to the xor gate

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which is used in a R-csla. It consists of 5 full adders were in each adder consists of two xor gates and 3 half adder and 3- & 4-bit BEC counters are used. Hence, the reduction in number of switching transistors reduces the power consumption as well as the power delay product (PDP).

[9] Design of 32-bit Carry Select Adder with Reduced Area

The area and delay of 8-bit, 16-bit, 32-bit and 64-bitbasic SQRT CSLA, SQRT CSLA with BEC logic are evaluated and compared with the proposed SQRT CSLA with add one circuit logic. The proposed adder takes less delay and area when compared with SQRT CSLA with BEC logic. It is also observed that in the proposed adder the reduction in area is very high with insignificant penalty in the delay when compared with traditional SQRT CSLA. As the input length is progressed, the area is decreased in the same proportion, but in the same proportion the delay penalty is not increased. Since the area in the proposed adder is very less, it is obvious that, the power consumption is also very less. But the delay of this proposed approach is more when compared with the original method.

III. PROPOSED WORK:

A conventional carry select adder (CSLA) is an RCA–RCA configuration that generates a pair of sum words and output-carry bits corresponding the anticipated input-carry (cin = 0 and 1) and selects one out of each pair for final-sum and final-output-carry. A conventional CSLA has less CPD than an RCA, but the design is not attractive since it uses a dual RCA. The main objective of SQRT-CSLA design is to provide a parallel path for carry propagation that helps to reduce the overall adder delay. The BEC-based CSLA involves less logic resources than the conventional CSLA, but it has marginally higher delay. In the existing designs, logic is optimized without giving any consideration to the data dependence. In this brief, we made an analysis on logic operations involved in conventional and BEC-based CSLAs to study the data dependence and to identify redundant logic operations. Due to optimized logic units, the proposed CSLA involves significantly less ADP than the existing CSLAs. Using the proposed CSLA design involves nearly less ADP and consumes less energy than that of the corresponding SQRT-CSLA. The proposed architectures have better performance in reduction of carry propagation delay than contemporary architectures. The proposed CSLA is based on the logic formulation and its structure. It consists of one HSG unit, one FSG unit, one CG unit, and one CS unit. The CG unit is composed of two CGs (CG0 and CG1) corresponding to input-carry “0” and “1”.

IV. CONCLUSION

We made an analysis on the logic operations involved in conventional CSLA and CSLA based on binary to excess-1 converter (CSLA-BEC) to study the data-dependency, and to find redundant logic operations. We have eliminated all the redundant logic operations of conventional CSLA, and proposed a logic formulation for CSLA. In the proposed scheme, the
carry-select operation is scheduled before the calculation of final-sum, which is different from the conventional approach. The proposed CSLA design involves significantly less area and delay than the recently proposed CSLA-BEC. Due to small carry-output delay, the proposed CSLA design is a good candidate for SQRT adder.

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