IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Vol. 8, Issue 6, June 2021

DOI: 10.17148/IARJSET.2021.8606

Performance Analysis of Asymmetrical Cascaded H-Bridge Multilevel Inverter Topology Using Soft Tool

Shivacharan Nayak[1], Dr. Sujatha Balaraman [2]

PG-Scholar, Department of Electrical Engineering, Government College of Technology, Coimbatore, India[1]

Associate Professor, Department of Electrical Engineering, Government College of Technology, Coimbatore, India[2]

Abstract: In past few years, multilevel inverter technology is blooming and expanding for its medium and high-power industrial applications. Basically, there are three main multilevel inverter topologies namely - Neutral Point Clamped, Flying Capacitor and Cascaded H-Bridge (CHB). Among them, Cascaded H-Bridge has become popular because of its modular design, simple control, reliability, availability and the absence of capacitor imbalance problem. This paper focuses on two Asymmetrical topologies- binary Asymmetrical and trinary Asymmetrical CHB topologies. Here, performance of these topologies is compared based on Total Harmonic Distortion (THD), efficiency and number of power devices requirement. In addition to that, a computer simulation using MATLAB/Simulink has been developed for seven level and nine level Asymmetrical CHB and their performances have been analysed. Consequently, higher level Asymmetrical CHB proves to be an apt alternative for future endeavours in renewable energy sources.

Keywords: Multilevel Inverter (MLI), Symmetrical, Asymmetrical MLI, Cascaded H-Bridge, Total Harmonics Distortion (THD).

I. INTRODUCTION

Over the last few years, technology is prevailing in all its form to every sector possible and for such exponential growth huge ac/dc power supply in industries and other areas is required [1][2]. For the purpose, inverter, a device that converts electrical power from dc to ac form using electronic circuits is employed.

Among varieties of inverters, multilevel inverter surpasses all due to the advantage of high-power quality waveforms, low electromagnetic compatibility. High performance a.c drive systems require high quality inverter output with low harmonic contents [3]. Conventional two-level inverters require high switching frequency to obtain a quality output voltage waveform whereas MLI could achieve higher power by using number of power switches with several low voltage dc sources [4][5]. It can also produce output voltage waveform in steps which is closer to sine wave and reduces total harmonic distortion.

Multilevel inverter is of three different types [6] :

- Diode Clamped Inverter
- Flying Capacitor Inverter
- Cascaded Inverter

Out of these, cascaded multilevel inverter has higher output voltage and power levels. It is one of the topologies used for drive application which meets the requirement such as high-power rating with reduced THD and switching losses.

There are two types of CHB-MLI:

- Symmetrical structure

When each cell of CHB-MLI is supplied by same magnitude of dc source then this structure is known as symmetrical structure [7].

- Asymmetrical structure

When each cell of CHB-MLI is supplied by unequal magnitude of dc source then this structure is known as symmetrical structure [8]. Asymmetrical cascaded MLI has a smaller number of DC source voltage and switches as compared to symmetrical cascaded MLI. An Asymmetrical cascaded MLI has an advantage of increased number of voltage levels for a given module counts [9][10]. Asymmetrical cascaded nine-level MLI and seven-level MLI were compared. On the basis of the obtained results, the most effective MLI is adopted that gives the reduced THD output and better performance for the resistive load.

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Vol. 8, Issue 6, June 2021

DOI: 10.17148/IARJSET.2021.8606

II. CASCADED H-BRIDGE MULTILEVEL INVERTER WITH UNEQUAL DC SOURCES

An Asymmetrical Cascaded Multilevel Inverter has DC sources of unequal magnitude of voltage. For our purposes, seven-level and nine-level Asymmetrical Cascaded MLI are considered [11]12]. In case of seven-level Asymmetrical Cascaded MLI, two unequal magnitude DC sources and eight power switches are used and three DC sources with twelve power switches are used in 9 level Asymmetrical Cascaded MLI. The basic power circuit for seven-level and nine-level Asymmetrical Cascaded MLI is shown in Fig. 1 and 2 respectively.

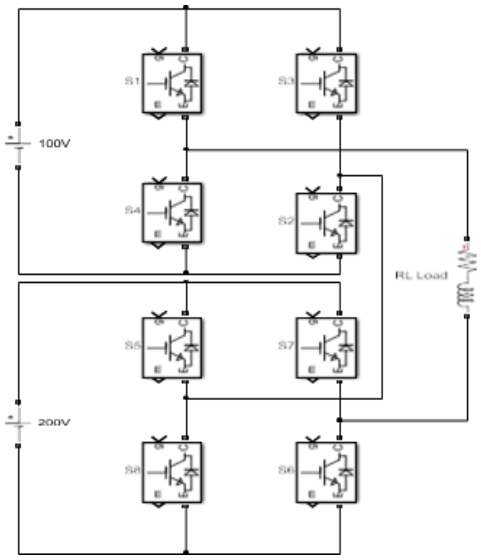

Fig. 1 Asymmetrical seven-level MLI

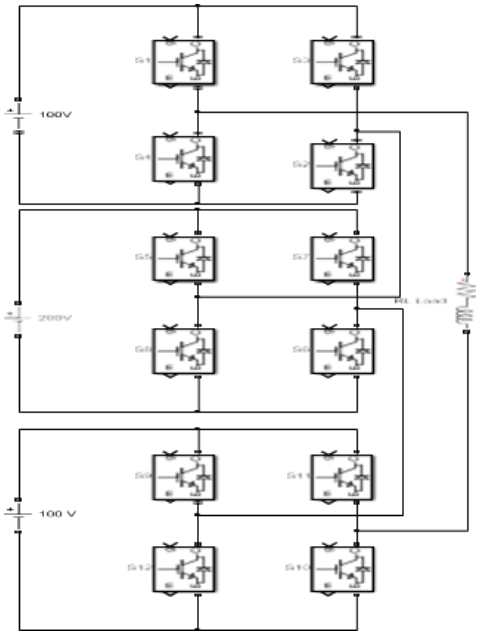

Fig. 2 Asymmetrical nine-level MLI

III. METHODOLOGY FOR SEVEN-LEVEL TOPOLOGY

The Asymmetrical cascaded seven level multilevel inverter has two DC sources and eight power switches magnitude of DC sources are 150V and 200V respectively. The sources are connected to two H-Bridge units which are cascaded in

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Vol. 8, Issue 6, June 2021

DOI: 10.17148/IARJSET.2021.8606

single phase. In an individual H-bridge the output voltage is $+V_{DC}$, 0 or $-V_{DC}$. Hence the desired output voltage for 9 level Asymmetrical CMLI are $-V_{DC,}$ $-2V_{DC}$, $-3V_{DC}$, 0, $+3V_{DC,}$ $+2V_{D,}$ $+V_{DC}$. In order to get desired output voltage, the power switches are turned ON and OFF in various combinations [13]. For maximum output voltage +3V; the switches S_1, S_6, S_5 and S_2 are ON and remaining switches are OFF at this time. Similarly, all voltage levels can be analyzed with the help of following Table I.

Table I: Switching pattern for Asymmetrical cascaded seven-level inverter

LEVELS SWITCHES	3V	2V	V	0	-V	-2V	-3V
S_1	1	0	1	0	0	0	0
S_2	1	1	1	0	0	1	0
S_3	0	0	0	0	1	0	1
S_4	0	1	0	0	1	1	1
S_5	1	1	1	0	1	0	0
S_6	1	1	0	0	0	0	0
S_7	0	0	1	0	1	1	1
S_8	0	0	0	0	0	1	1

IV. METHODOLOGY FOR NINE-LEVEL TOPOLOGY

The Asymmetrical cascaded nine-level multilevel inverter has three DC sources and twelve power switches magnitude of DC sources are 100V, 200V and 100V respectively. The sources are connected to three H-Bridge units which are cascaded in single phase. In an individual H-bridge the output voltage is $+V_{DC}$, 0 or $-V_{DC.}$ Hence the desired output voltage for 9 level Asymmetrical CMLI are $-V_{DC,}$ $-2V_{DC}$, $-3V_{DC,}$ $-4V_{DC}$, 0, $+4V_{DC}$, $+3V_{DC,}$ $+2V_{DC,}$ $+V_{DC}$. In order to get desired output voltage, the power switches are turned ON and OFF in various combinations [14]. For maximum output voltage +4V; the switches S_1, S_{10}, S_9, S_6, S_5 and S_2 are ON and remaining switches are OFF at this time. Similarly, all voltage levels can be analyzed with the help of following Table II.

Table II: Switching pattern for Asymmetrical cascaded nine-level inverter

LEVELS SWITCHES	4V	3V	2V	V	0	-V	-2V	-3V	-4V
S_1	1	1	0	1	0	0	0	0	0
S_2	1	1	1	1	0	0	1	0	0
S_3	0	0	0	0	0	1	0	1	1
S_4	0	0	1	0	0	1	1	1	1
S_5	1	1	1	0	0	0	0	0	0
S_6	1	1	1	1	0	1	0	0	0
S_7	0	0	0	0	0	0	1	1	1
S_8	0	0	0	1	0	1	1	1	1
S_9	1	0	0	0	0	0	0	0	0
S_{10}	1	1	1	1	0	1	1	1	0
S_{11}	0	0	0	0	0	0	0	0	1
S_{12}	0	1	1	1	0	1	1	1	1

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Vol. 8, Issue 6, June 2021

DOI: 10.17148/IARJSET.2021.8606

V. CONTROL STRATEGIES FOR SWITCHING

Multilevel inverter has to render a staircase waveform by using the modulation techniques for controlled output voltage [14] [15]. There are variety of modulation techniques available one out of such techniques are, level shifted pulse width modulation(LS-PWM) which is considered as the most efficient method. The LS-PWM is classified into: a) in-phase disposition, b) alternative phase opposite disposition (APOD) c) phase opposite disposition (POD) [15]. Here phase disposition (PD) modulation technique is utilized. The reference signal has 50 HZ frequency and carrier waves have 2KHZ to 3KHZ frequency. A triangle generator is employed in order to get carrier wave. The modulation index is defined as

Modulation index = V_{ref}/V_{car}

where V_{ref} is reference voltage and V_{car} is carrier. And it is taken as 0.97.

VI. SOFT IMPLEMENTATION

The complete result is observed in MATLAB/SIMULINK .The complete simulation circuit for Asymmetrical 7 and 9 level MLI with resistive load are shown in Fig. 3 and 4.

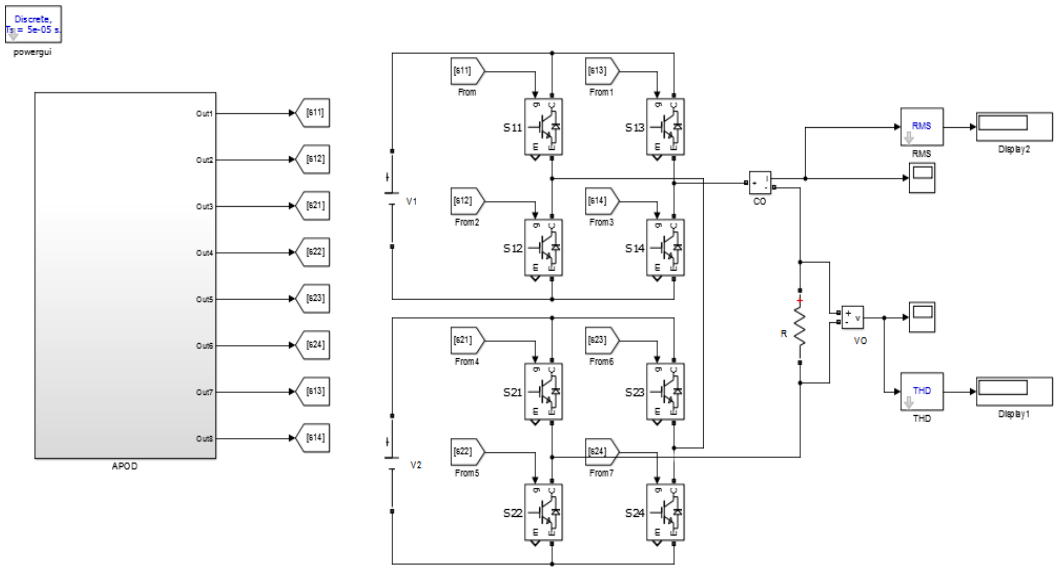

Fig. 3 Asymmetrical seven-level MLI

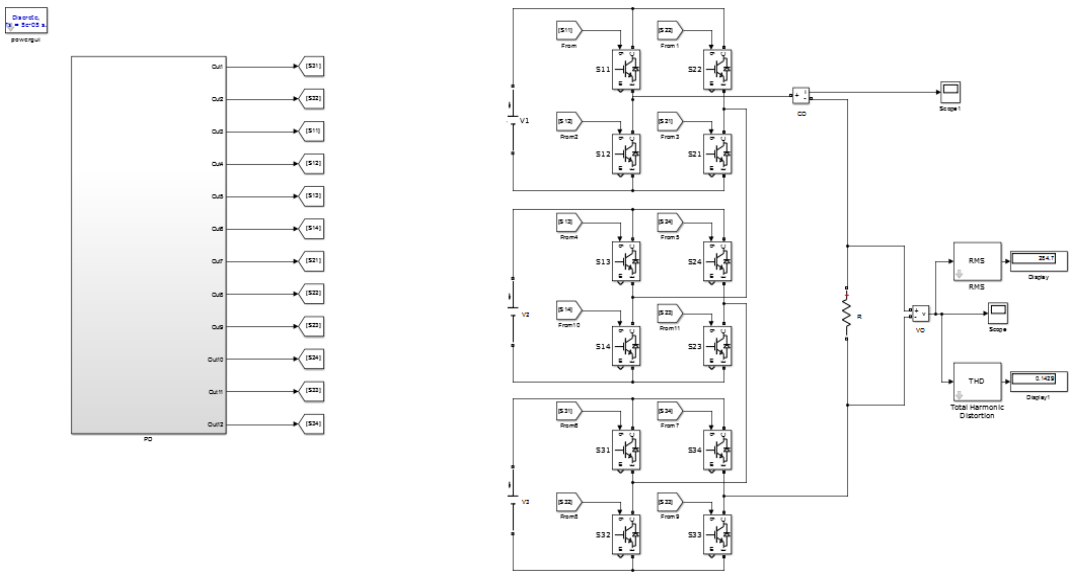

Fig. 4 Asymmetrical nine-level MLI

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Vol. 8, Issue 6, June 2021

DOI: 10.17148/IARJSET.2021.8606

VII. SIMULATION RESULTS AND OUTCOMES

The performance analysis has been carried out for seven-level and nine-level Asymmetrical inverters with resistive load using following parameters specified in Table IV.

Table III: Various input parameters for seven-level and nine-level Asymmetrical Multilevel Inverter

Parameters	7-Level Asymmetrical Multilevel Inverter	9-Level Asymmetrical Multilevel Inverter
Voltage V_1 V_2 V_3	350 V 150 V 200 V	400 V 100 V 200 V 100 V
Frequency	50 Hz	50 Hz
Load(R)	10Ω	10Ω

The output voltage waveform of seven-level Asymmetrical cascaded MLI with resistive load is shown in Fig. 5.

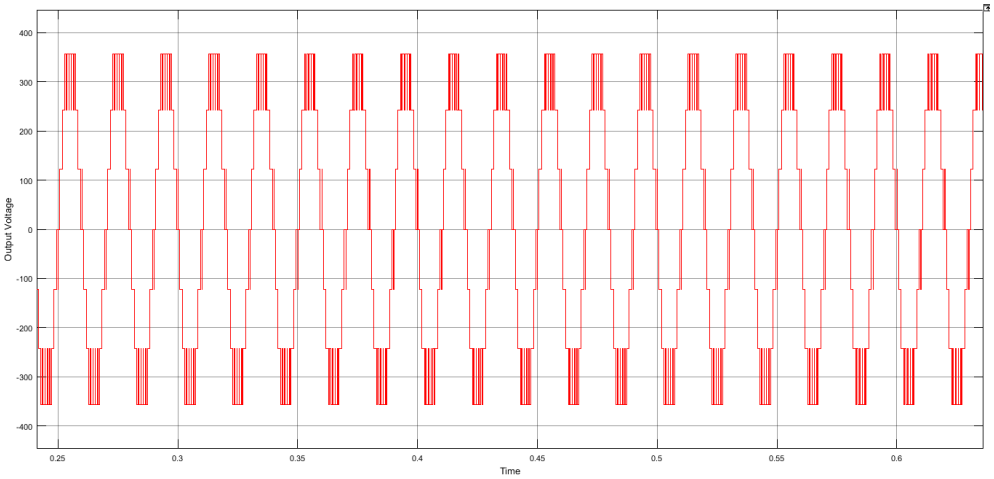

Fig. 5 Output voltage waveform for seven-level Asymmetrical Multilevel Inverter

The output current waveform of seven-level Asymmetrical cascaded MLI with resistive load is shown in Fig. 6.

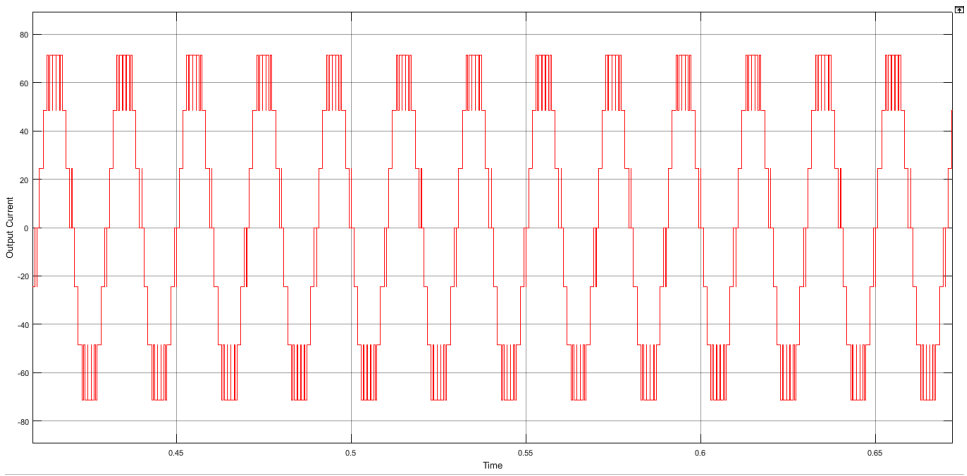

Fig. 6 Output current waveform for seven-level Asymmetrical Multilevel

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Vol. 8, Issue 6, June 2021

DOI: 10.17148/IARJSET.2021.8606

The output voltage waveform of nine-level Asymmetrical cascaded MLI with resistive load is shown in Fig. 7.

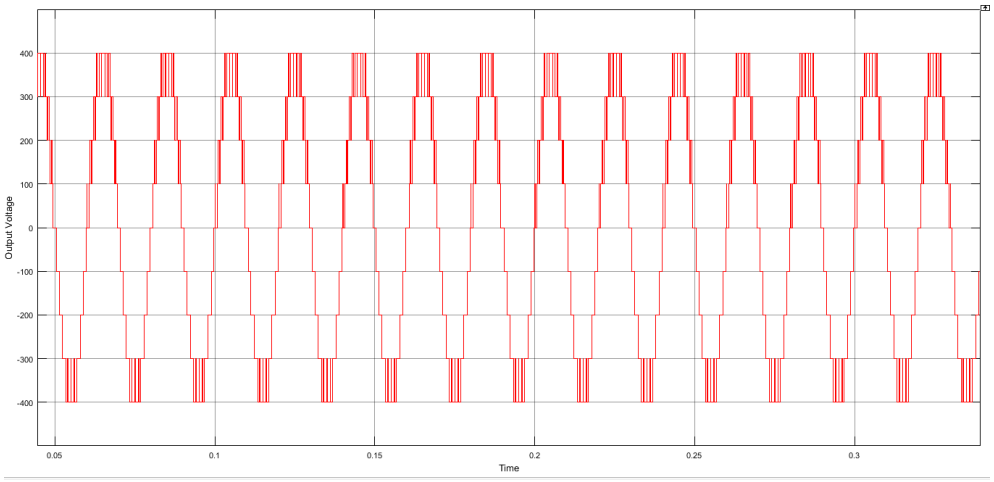

Fig. 7 Output voltage waveform for nine-level Asymmetrical Multilevel Inverter

The output current waveform of nine-level Asymmetrical cascaded MLI with resistive load is shown in Fig. 8.

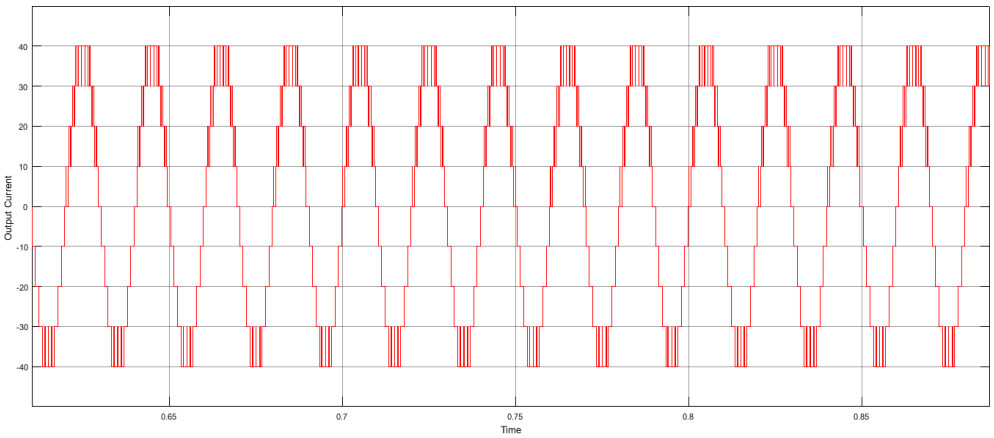

Fig. 8 Output current waveform for nine-level Asymmetrical Multilevel Inverter

The corresponding FFT analysis of voltage waveform of seven-level Asymmetrical cascaded MLI with resistive load is shown in Fig. 9.

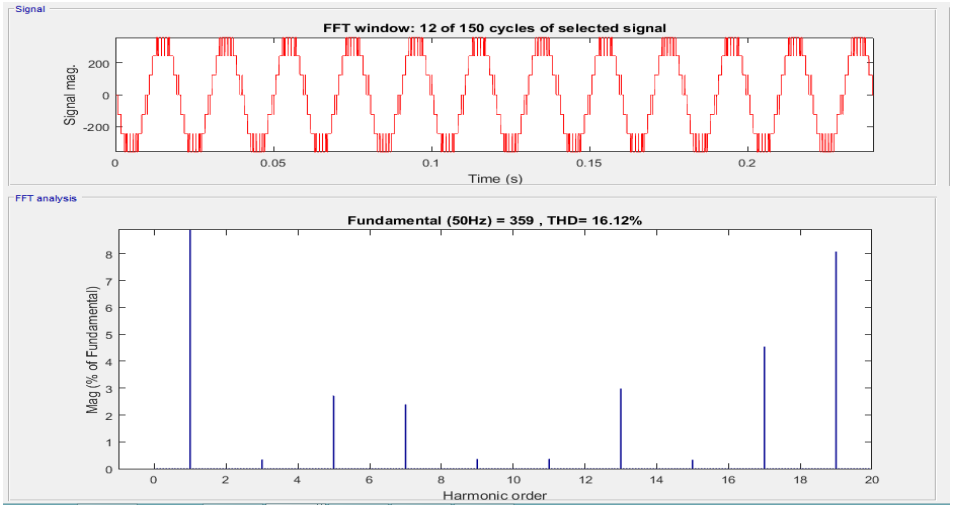

Fig. 9 FFT analysis of voltage waveform of seven-level Asymmetrical Multilevel Inverter

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology
Vol. 8, Issue 6, June 2021

DOI: 10.17148/IARJSET.2021.8606

The corresponding FFT analysis of current waveform of seven-level Asymmetrical Multilevel Inverter is shown in Fig. 10.

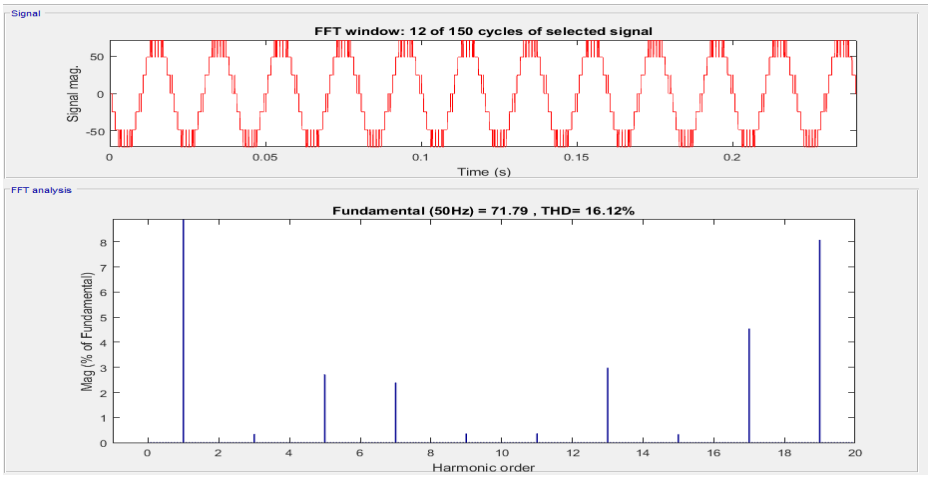

Fig. 10 FFT analysis of current waveform of seven-level Asymmetrical Multilevel Inverter

The corresponding FFT analysis of voltage waveform of nine-level Asymmetrical cascaded MLI with resistive load is shown in Fig.11.

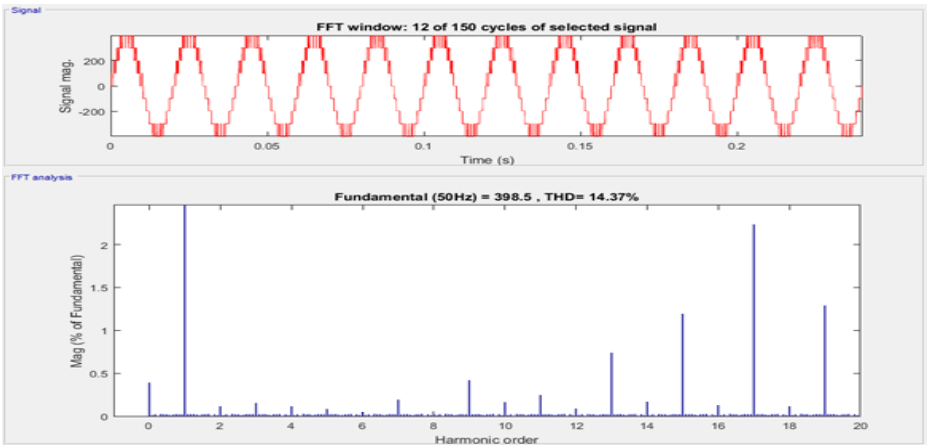

Fig. 11 FFT analysis of voltage waveform of nine-level Asymmetrical Multilevel Inverter

The corresponding FFT analysis of current waveform of nine-level Asymmetrical Multilevel Inverter is shown in Fig.12.

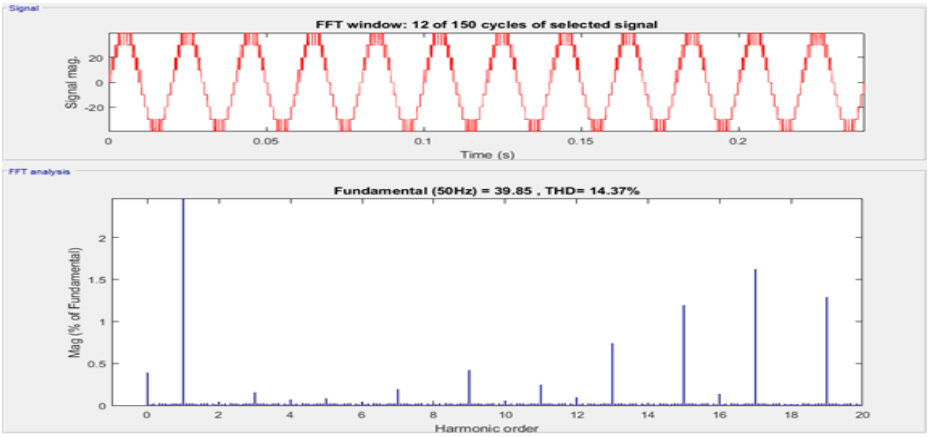

Fig. 12 FFT analysis of current waveform of nine-level Asymmetrical Multilevel Inverter

IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Vol. 8, Issue 6, June 2021

DOI: 10.17148/IARJSET.2021.8606

The Table IV elucidates the simulation results of seven-level and nine-level Asymmetrical Multilevel Inverter. The output efficiency procured by seven-level Asymmetrical Multilevel Inverter and nine-level Asymmetrical Multilevel Inverter is 85.46% with 16.12% THD and 94.9% with 14.37% THD respectively. Overall, the voltage spectrum is much better for nine-level inverter topology than seven-level Asymmetrical Multilevel Inverter.

Table IV: Comparison between seven-level and nine-level Asymmetrical Multilevel Inverter

Parameters	7-level Asymmetrical Multilevel Inverter	9-level Asymmetrical Multilevel Inverter
No. of DC sources	2	3
No. of switches	8	12
Fundamental Frequency(Hz)	50	50
DC Source Voltage(V)	350	400
Voltage levels	7	9
Load Voltage (RMS)	256.4	284.7
Voltage THD (%)	16.12	14.37
Output Efficiency (%)	85.46	94.9

VIII. CONCLUSION

The performance analysis of seven-level Asymmetrical and nine-level Asymmetrical CHB-MLI with multiple H-bridges is carried out with resistive load. MATLAB/Simulink models are developed for both the topologies along with line THD. The proposed model yields 14.17% THD for seven-level AMLI and 16.37% THD for nine-level AMLI without using any filter circuit. From the simulation results it is observed that the generated voltage spectrum is very much improved with nine-level inverter topology. Among the two configurations, it is evident that the nine-level Asymmetrical CHB-MLI requires less number of switches and dc sources and generates high quality voltage with minimum harmonics. The proposed inverter asymmetrical topology is more suitable for solar photovoltaic applications.

REFERENCES

[1]. C. Dhanamjayulu And S. Meikandasivam. (2018). " *Implementation and Comparison of Symmetric and Asymmetrical Multilevel Inverters for Dynamic Loads*". IEEE Acess,Vol.6, pp.738-7-46.
[2]. Y. Suresh and A. K. Panda. (2013).``*Investigation on hybrid cascaded multilevel inverter with reduced DC sources"*. Renew. Sustain. Energy Rev., vol. 26, pp. 49-59.
[3]. C. I. Odeh and D. B. N. Nnadi. (2013). ``*Single-phase, 17-level hybridized cascaded multi-level inverter"*. Electr. Power Compon. Syst., vol. 41, No. 2, pp. 182- 196.
[4]. J. Rodriguez, J-S. Lai, and F. Z. Peng. (2002). *"Multilevel inverters: A survey of topologies, controls, and applications"*. IEEE Trans. Industrial Electronics, Vol. 49, No. 4, pp.724-738.
[5]. L. M. Tolbert, F. Z. Peng, and T. G. Habetler. (1999). *"Multilevel converters for large electric drives"*. IEEE Trans. Ind. Appl., Vol. 35, No. 1, pp. 36-44.
[6]. S. Kouro, M. Malinowski, *et al.* (2010). *"Recent advances and industrial applications of multilevel converters"*. IEEE Trans. Ind. Electron., vol. 57, No. 8, pp. 2553–2580.
[7]. Farid Khoucha, *et al.* (2011). *" A comparison of symmetrical and Asymmetrical three-phase H-bridge multilevel inverter for DTC induction motor drives"* IEEE Trans. on Energy Conversion, vol.26, no. 1.
[8]. M. Malinowski, K. Gopakumar, *et al.* (2010). *"A survey on cascaded multilevel inverters"*. IEEE Trans. Ind. Electron., vol. 57,No. 7, pp. 2197–2206.
[9]. F. Z. Peng and J. S. Lai. (1997). *"Multilevel cascade voltage-source inverter with separate DC source"*. U.S. Patent 5 642 275.
[10]. H. Abu-Rub, J. Holtz, and J. Rodriguez. (2010). *"Medium-voltage multilevel converters–State of the art, challenges, and requirements in industrial applications"*. IEEE Trans. Ind. Electron., vol. 57, No. 8, pp. 2581–2596.
[11]. Brendan Peter McGrath, Donald Grahame Holmes. (2002). *"Multicarrier PWM strategies for multilevel inverters"*. IEEE Trans. On Ind.l Electronics, vol. 49, No. 4.
[12]. T. A. Meynard, H. Foch. (1992). *"Multilevel conversion: High voltage choppers and voltage source inverters"*. IEEE- PESC Conference Record, pp.397-403.
[13]. A.Nabae, I. Takahashi, H.Akagi. (1981). *"A new neutral-point clamped PWM inverter"*. IEEE Trans. Ind. App. vol. IA-17, No.5, pp 518-52.
[14]. Juan Dixon, Javier Pereda. (2010). *"Asymmetrical multilevel inverter for traction drives using only one dc supply"*. IEEE Trans. On Vehicular Technology, vol. 59, No. 8.
[15]. L. G. Franquelo, J. Rodriguez, *et al.* (2008). *"The age of multilevel converters arrives"*. IEEE Industrial Electronics Mag., Vol. 2, No. 2, pp. 28-39.