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Literature Review on "Clock Optimization for High Speed Synchronous Circuits".

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Abstract: In this paper, we made an analysis on various clock distribution networks (CDN) and algorithms which are used to reduce the clock skew in the circuits to study the various delays associated in the circuit and also the clock parameters which we need considered. Some of the CDN concepts emphasize on the distance of the clock buffers from the clock source in order to reduce the clock skew by maintaining clock sinks at same distances from the clock source and some of the CDN concepts involve algorithms which help in developing a clock network which supplies clock to the clock buffers which are already placed at a certain positions and some of the concepts also involve delay models (such as Elmore delay model) in order develop a CDN with minimal clock skew. To study and as well as implement our proposed methodology which particularly emphasizes about clock skew we took the pipelining process into consideration to develop an efficient method to tackle the problems of clock skew, so in this paper we have also studied and made analysis on pipelining process. Many CDNs have reduced clock skew but not eliminated so we have proposed a methodology which helps in utilizing clock skew to increase the speed of the circuit.

Keywords: Clock, CDN, clock skew, clock buffer, pipelining.

I. INTRODUCTION

The requirement for high speed digital circuits is increasing day by day and optimization with respect to the supply of clock can be one way of increasing the speed of the circuit i.e., in a synchronous digital system, the clock signal is used to define a time reference for the movement of data within that system which leads to proper synchronization of the operation(s) which is being carried out by the circuit. Since this function is vital to the operation of a synchronous system, much attention has been given to the characteristics of these clock signals and the networks used in their distribution. Clock signals are often regarded as simple control signals; however, these signals have some very special characteristics and attributes. Clock signals are typically loaded with the greatest fanout, travel over the longest distances, and operate at the highest speeds of any signal, either control or data, within the entire system. Since the data signals are provided with a temporal reference by the clock signals, the clock waveforms must be particularly clean and sharp. Finally, any differences in the delay of the clock signals i.e., clock skew can severely limit the maximum performance of the entire system as well as create catastrophic race conditions in which an incorrect data signal may latch within a register. Most synchronous digital systems consist of cascaded banks of sequential registers with combinational logic between each set of registers (pipelining process). Local timing requirements are satisfied by the careful insertion of pipeline registers into equally spaced time windows to satisfy critical worst case timing constraints. The proper design of the clock distribution network further ensures that these critical timing requirements are satisfied and that no race conditions exists .With the careful design of the clock distribution network, system level synchronous performance can actually increase, surpassing the performance advantages of asynchronous systems. In synchronous systems, each data signal is typically stored in a latched state within a bi stable register awaiting the incoming clock signal, which determines when the data signal leaves the register. Once the enabling clock signal reaches the register, the data signal leaves the bi stable register and propagates through the combinatorial network (combinational logic circuit) and, for a properly working system, enters the next register and is fully latched into that register before the next clock signal appears. Thus, the delay components that make up a general synchronous system are composed of the following three individual subsystems memory storage elements, logic elements, clocking circuitry and distribution network. Many clock distribution networks have been developed to reduce and eliminate the clock skew and most of these CDNs have succeeded in reducing the clock skew but we can still encounter the presence of clock skew, so it is required to develop a CDN which helps in utilizing the clock skew to increase the speed or performance of the circuit and the proposed methodology ensures in developing such an effective CDN.

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II. LITERATURE SURVEY

[1] Clock skew scheduling for improved reliability via quadratic programming

In digital synchronous circuits, clock skew plays an important role in the performance aspect of the circuit and it is important to note that developing an effective CDN which helps in reducing the clock skew and maintaining it under the tolerable value is a very important requirement, in this paper an effective and an optimal clock skew scheduling scheme is proposed, in order to help in developing a CDN which aims for zero clock skew in the synchronous VLSI circuits. The clock skew scheduling is formulated as a constrained quadratic programming. The range of the clock skew with respect to each of the local data path which is considered to be a 'permissible range' plays an important role in this formulation. To evaluate reliability, a quadratic cost function is introduced as the Euclidean distance between the ideal schedule and a given practically feasible clock schedule. By following this type of clock scheduling we can still encounter the presence of clock skew and the process is bit complex and due to the advancements in the EDA tools we can develop process which are simpler. By ensuring the same distance between the clock source and the respective clock sinks it cannot be guaranteed that the skew will be eliminated.

[2] Clock Distribution Networks in Synchronous Digital Integrated Circuits

Clock distribution networks are one of the largest networks or interconnects present inside an IC and they play a very important role in distribute an very important synchronizing signal and a time reference signal called as clock signal to the respective sequential circuits or clock buffers, so it is very important to develop an efficient and effective CDN in order to enhance the performance of the digital circuits. In this paper various CDNs which are basic and effective are proposed and in detail information of these CDNs are provided. All the theoretical information with respect to these CDNs are provided but practical information with respect to these CDNs are not covered and the requirement for information regarding the implementation or practical approach in developing these CDNs is considerably important.

[3] Clock Distribution Design in VLSI Circuits - an Overview

Clock distribution networks are networks in Digital circuits or VLSI circuits which are assigned with certain important responsibility [2] that need to be taken care of and while accomplishing or taking care of these responsibility there are certain parameters with respect to the timing requirements that need to be considered. In this paper various timing requirements that need to be considered while developing or designing a CDN are discussed and the details regarding how to satisfy these timing requirements are provided in the form of equations and timing diagram. In this paper the topic of clock distribution network is again divides into 4 subtopics and the information provided regarding these subtopics are in detail and clear and future trends with respect to these CDNs are discussed. The information is more theoretical and it is important to specify the constraints encountered during the practical approach of this designing process of CDNs

[4] A Synchronous Approach for Clocking VLSI Systems

This study describes a synchronous clocking solution for VLSI systems that are organized as distributed systems. The disadvantages of the self-timed approach are avoided with this solution. These VLSI systems are made up of modules that depict synchronous areas enabled or driven from their own fast clocks and are linked together by a synchronous communication mechanism with a slow clock. Using a single and accurate clock generator, the systems are structured as dispersed systems. These design methods are quite similar to those used in the development of existing distributed systems that use synchronous modules and asynchronous communication. The dynamic phase adjustment mechanism included into each internal module prevents metastability from being induced by propagation delays into the clock distribution system. This VLSI system is not actually a multiclock device because all of its internal clocks are created from a single clock generator, this solution does not contradict the theoretical conjectural insolvability of metastability. This kind of mechanism might involve more number of interconnects or routing congestion in circuits which are small in size.

[5] Design and Analysis of a Hierarchical Clock Distribution System for Synchronous Standard Cell/Macrocell VLSI

The synchronous clock distribution problem in VLSI is described in this study, as well as approaches for solving it, a Hierarchical design technique for decreasing clock skew in a VLSI circuit, in particular. This method has the advantage of decreasing chip-level clock skew. In addition, the overall clock latency between the input pin and the sequential registers is minimized and the RC time constants are lowered, resulting in reduction of overall clock delay and skew. The drawback is that transconductances of transistors, unlike interconnect impedances, are extremely sensitive to both process and environmental fluctuations (e.g., temperature, radiation, etc.). As a result, under worst-case and best-case scenarios, the performance of an ideally designed clock distribution system constructed under steady state conditions will tend to vary. This kind of clock distribution system has been used in an example, and the process for implementing it has been discussed.

[6] Clock Distribution in General VLSI Circuits

This study provides a clock routing technique for a universal VLSI circuit with functional units of varying sizes and placements that largely minimizes clock skew. An additional goal is to decrease total network delay. Based on the

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study of RC trees, the clock distribution network is created. The delay observed from the clock entry point of a circuit to all modules inside the circuit is almost equal in the networks so constructed. Clock skew is caused by unequal path lengths and active elements in a clock distribution network, whereas excessive delay is caused by the network's very long signal pathways. This paper proposed a clock routing strategy that addresses a number of real-world layout issues. In comparison to previous research in this field, this study employs a more accurate delay model that replicates the physical tree structure of a distribution network. Buffer fan out is taken into account, as well as the flexibility with which those buffers are placed. The aim of the research was to reduce the clock skew, which has been accomplished, but the clock skew still exists therefore it is appropriate and important to develop a concept of clocking which is capable of making benefit out of the clock skew.

[7] Zero skew clock net routing

In this study, a new clock net routing technique called ZSTM is demonstrated. It is based on a zero skew merging method and balanced partitioning. To lower the overall wire length, the balanced partition uses the minimal sum of diameter as the cost function. The delayed merging method creates a segment tree that preserves all conceivable clock tree layouts at the same cost. In this paper, a comparative analysis between the MMM algorithm and ZSTM algorithm is provided and considerable amount of reduction in delay, wire length and cost can be seen, but we can experience that the algorithm is relatively bit more complex. Might cause routing congestions in smaller circuit (regional clock distribution) and might not be effective in unsymmetrical circuits.

[8] Design of Low Power & High Performance Multi Source H-Tree Clock Distribution Network

Optimization of clock distribution networks is critical in creating low-power and high-performance designs as the VLSI industry goes towards implementing designs on lower technology nodes. In this paper, design and implementation of Multi Source Clock Tree Synthesis (MSCTS) with a symmetric H-Tree is discussed. Multiple clock sources in the design reduce clock latency and skew, resulting in fewer buffers being included to optimize hold timing, and so improving total power dissipation and clock QoR metrics. Therefore latency, skew, and power consumption are all reduced as compared to a traditional clock distribution network.. Though multi source clocking might show improved results it might require comparatively more space and might cause routing congestion and increase in the complexity of the network.

[9] Wave-Pipelining: A Tutorial and Research Survey

Wave-pipelining has gone from a theoretical aberration to a viable, albeit difficult, VLSI design process due to the combination of high-performance integrated circuit (IC) technologies, pipelined architectures, and advanced computer-aided design (CAD) tools. This paper includes a tutorial on wave-pipelining principles, as well as an overview of wave-pipelined VLSI chips and CAD tools for wave-pipelined circuit synthesis and analysis. Wave-pipelining is a high-performance circuit design technique that uses no intermediate latches or registers to execute pipelining in logic. Wave pipelining might cause additional challenges while testing the circuit for delays, dynamic power and clock tuning techniques which are not yet widely used can favor wave pipelining. Since it is mentioned in an explicit manner that wave pipelining might pose challenges during the testing of circuit with respect to delay, it is appropriate to infer that usage of conventional pipelining method is more advisable when testing clocking schemes which involve timing analysis as seen in our proposed methodology.

[10] Design and implementation of 8-bit Vedic multiplier using mGDI technique

It is clear that area, power and delay are important parameters in VLSI domain which involved in continuous enhancement due to the requirements posed by the present fashion. In this paper an 8 bit Vedic multiplier is constructed using mGDI technique or modified gate diffusion input technique. It is clear by the comparative analysis provided in this paper that 8 bit Vedic multiplier constructed using mGDI technique has an upper hand when it comes to power, area and delay when compared to 8 bit Vedic multiplier built using CMOS technique. So it is advisable to use this circuit as a test circuit for testing clock scheme that is mentioned in the proposed methodology.

III. PROPOSED WORK

In digital synchronous circuits, clock skew plays an important role in the performance aspect of the circuit and it is important to note that developing an effective CDN which helps in tackling the problems involved by the occurrence of clock skew effectively is very important. The proposed clock distribution network(or a scheduling scheme) involves the process of pipelining a complex combinational logic circuit (Multiplier) and supplying clock from a single clock source to the respective registers which are included due the pipelining process, the pipelined circuit is again divided into 4 symmetrical sector buffers and the clock is supplied to each of these four sectors from the clock source through a clock distribution network which ensures zero skew and later the clock received by each of these sector buffers are then distributed among of the registers(clock sinks) present in each of these sectors using a clock distribution network which follows a clock scheduling scheme that resembles an unconstrained clock distribution network, this method of clock scheduling involves a delay optimization circuit consisting of inverters or buffers which helps in utilizing the skew as a beneficial parameter which helps in increasing the performance of the circuit. Initially a multiplier (test

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circuit is divided into a number of smaller combinational logic circuits using pipelining technique. Schematic of the pipelined multiplier is designed using Cadence Virtuoso tool. After creating the schematic, a layout of the pipelined circuit (test circuit) is designed. The proposed clock synthesis is implemented to the layout that is designed. Later the existing conventional clock distribution network is implemented for the same multiplier circuit (test circuit). Later post layout synthesis is performed on both the designs (CDNs) and their respective outputs are compared.

IV. CONCLUSION

We made an analysis on the basic clock scheduling methods and also on the clock distribution networks which follows those clock scheduling schemes and it is seen that most of the CDNs have tried to eliminate clock skew but yet most of those CDNs have achieved in reducing the clock skew but not eliminated. therefore by seeing the persistent presence of clock skew it is appropriate to infer that we need to develop an efficient clocking method which helps in making benefit out of the clock skew rather than trying to eliminate the clock skew and we have proposed a methodology which helps in using clock skew to enhance the performance of the circuit in an effective manner. We have also performed analysis on pipelining techniques and also on Vedic multiplier, which is our test circuit, to ensure that we can implement the proposed methodology in and efficient manner.

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