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Simulation of Graded Channel Double Gate Junctionless Transistor for Low Power and High Performance

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Abstract: This paper proposes a novel structure of n-MOS Graded Channel Double Gate Junctionless transistor (GC DG JLT). Using TCAD the design and characteristics of GC DG JLT are compared with SC DG transistor with equal dimensions. From the results, it is observed that as the side gate voltage of GC DG JLT is increased, the surface potential also increases which ultimately increases the current driving capability. SC DG transistor has a prominent hot electron effect compared to GC DG JLT as the electric field distribution is more than 50% at drain side in SC DG transistor. It has been also observed that on- state current of GC DG JLT is more than that of the SC DG transistor. Threshold voltage roll-off is also less in GC DG JLT when the side gate length is varied. For the 20 nm main channel length, the DIBL is improved by 33% for the GC DG JLT compared to SC DG transistor. The Transconductance of the GC DG JLT is three times more than that of SC DG transistor at a gate voltage of 0.6V. The Sub-threshold slope of GC DG JLT is improved to 53% compared to SC DG transistor when the side gate length is length is 30nm and main gate length is 20 nm. Gm/IDS is the minimum in the saturation region which mean that drain to source current is most in the saturation region for the GC DG JLT.

Keywords: Graded channel DG JLT (GC DG JLT), Shielded channel DG transistor (SC DG), Drain induced barrier lowering (DIBL), Transconductance (Gm), Short channel effects (SCE), Sub- threshold Slope (SS)

I. INTRODUCTION

Fundamental building blocks of all the modern electronic devices are transistors [1]. The Semiconductor industry successfully following Moore's law by doubling the no of transistors on the IC every 18 months. The ITRS (International Technology Road Map of Semiconductor) predicted that the conventional metal oxide field effect transistor will reach sub- 10nm dimensions in 2018[2].

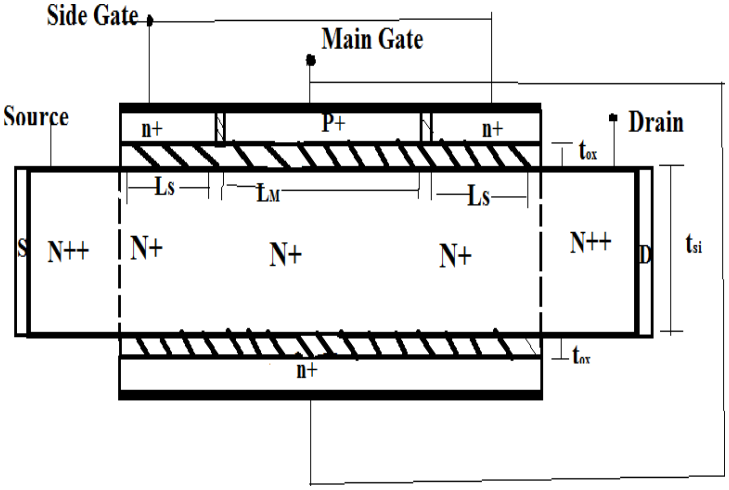

Fig. 1 n-channel GC DG JLT

Device Miniaturization is important to give high-speed at low cost. Nano scale MOSFET give high device density, low power consumption and high speed, these three things are very important for the progress of electronics [3]. Miniaturization of conventional MOSFET is challenging due to loss of control of gate over the channel carriers. An alternative to this, multi-gate devices has been developed which has better electrostatic control of the charges which gives better control over the SCE's but creation of ultra- sharp p-n junction needed which is

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more complex so the Junctionless transistor is proposed[4]. The novel concept of Junctionless transistor is proposed in 2009 by J.P.Collinge and in the year 2010 it is demonstrated that challenges in the fabrication process of creating ultra-sharp and abrupt junctions of conventional MOSFET's is eliminated [5]. Junctionless transistor is also termed as gated resistor or vertical FET [6]. As per the predictions of ITRS, CMOS technology is scaled down to sub-nanometer region has short channel effects such as large drain induced barrier lowering, poor sub-threshold slope swing, threshold voltage roll off, increased leakage current [6]. Power dissipation in the CMOS IC is one of the big problems in the scaling down the device issipation can be effectively reduced by reducing supply voltage and lowering the threshold voltage also increase the performance of the CMOS devices [7]. Active power dissipation is proportional to the square of the supply voltage, in the last 20 years the supply voltage is reduced up to 1.1V.The slope of the drain current to the gate voltage curve in the sub-threshold operation gives Sub- threshold slope. For the conventional MOSFET, the SS should be less than 60mV/decade and it is difficult to get desired SS at supply voltage less than 0.6V, but it is possible to get in JLT [8]. Unlike the conventional MOSFET, the channel region of Junctionless transistor is heavily and uniformly doped from source to drain region which causes high scattering mechanism to lead to almost zero electric fields at the center of the channel which is beneficial to the mobility of charge carriers [9]. Since there are no p-n junctions in the Junctionless transistor it has better electrical properties than that of conventional MOSFET [10] and it eliminates the diffusion of impurities and formation of sharp doping profile formation [11]. Due to thermal diffusion of S/D dopant into the channel, the conventional MOSFET have shorter effective channel length while in the Junctionless transistor the effective channel length is longer because of work function difference between gate electrodes and channel pushes depletion region away from the gate towards the S/D side. Due to work function difference between the gate electrode and channel semiconductor, at the off state (gate voltage is 0V) the channel is fully depleted with carriers, and when the gate voltage is greater than the threshold voltage but less than flat band voltage conduction through the center of the channel takes place and further gate voltage is increased beyond flat band voltage, mobile carriers density increased at the surface resulting surface current conduction [6]. Junctionless transistor is a strong candidate for future decananometer MOSFET applications [12]. Junctionless transistor has excellent turn on and sub-threshold characteristics along with low off current [13]. But heavily doped channel affects the carrier mobility and directly on the drive current and transconductance of JLT, so dual-material gate JLT proposed and studied and came to know that dual material JLT have improved carrier transport efficiency and transconductance along with suppressed SCE's [14]. In this paper, we propose a new novel structure named as Graded channel DG JLT by combining the advantages of JLT and duel- material gate structure and their characteristics are investigated using TCAD simulations [15]. COGENDA TCAD simulation incorporated drift diffusion model, the full energy balance model, carrier recombination, generation model, Fermi Dirac statics, band-to-band tunneling, and impact ionization models with mobility models. In the GENIUS code, the default low field mobility model is Analytic Mobility model for all materials [15].

DEVICE STRUCTURE AND SIMULATION

TABLE I: Device / Process Parameters

Parameters	**SC DG transistor (Orouji &Kumar,2005)**	**GC DG JLT**
Channel doping (cm-3)	N_D=1*10^{19} N_A=1*10^{16}	N+=0.4*10^{18} N++=1*10^{19}
Channel thickness (nm)	10nm	10nm
Channel length (nm)	L_M=20,L_S=10	L_M=20,L_S=10
Gate oxide thickness (nm)	1nm	1nm
Gate work function (eV)	P^+poly gate=5.1 N^+poly gate=4.9	P^+poly gate=5.1 N^+poly gate=4.9
Length of source and drain region (nm)	10nm	10nm

The structure of the proposed device Graded channel DG JLT (GC DG JLT) is explained here. The simulation is done by using COGENDA TCAD two-dimensional device simulators [16]. Fig.1 shows the structure of the proposed GC DG JLT. For the main gate p+ polysilicon is used while for side gate and bottom gate n+ polysilicon is used. The Main channel length is kept 20nm and channel side gate length is kept 10nm. The source and drain

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side region are heavily doped with a doping concentration of $1*10^{19}$ cm^{-3} than that of the channel region which is doped with $0.4*10^{18}$ cm^{-3}. Main gate and side gate oxide thickness is 1 nm and diffusion barrier is about 1 nm.

II. RESULTS AND DISCUSSION

The proposed Graded Channel DG JLT is simulated for the channel potential and position in the channel with different side gate voltages. The plot of the surface potential vs. position in the channel is shown in the Fig.2. Position in the channel is showed along X-axis and surface potential is showed along Y axis of the plot. Side gate voltage affects the surface potential of the channel [17]. As the side gate voltage is 0 V, the surface potential of the channel is least and when the side gate voltage is increased, the surface potential also increases and eventually the current driving ability of the channel also increases [18]. It is seen that as the side gate voltage is increased above the 0 V, the surface potential edges shifts towards the channel.

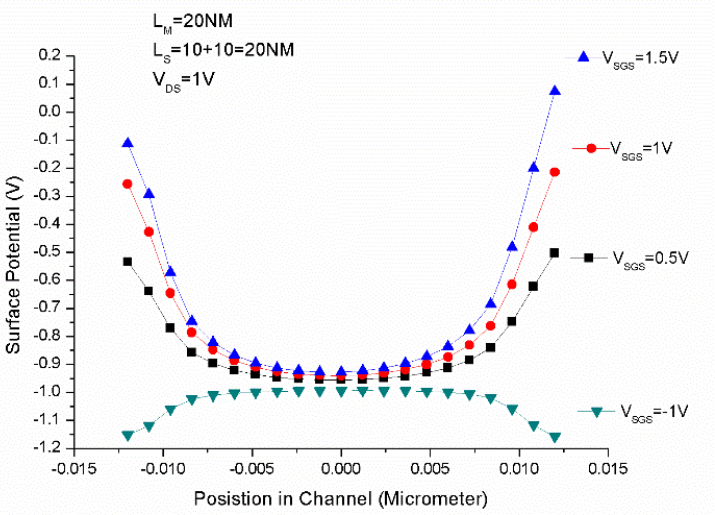

Fig. 2 Channel potential variation for different side gate biases of GC DG JLT.

Electric field distribution along the channel is shown in Fig 3. From the figure, it is observed that SC DG transistor have the high electric field at the drain side and it is about more than 50 % as compared with the Graded channel DG JLT. From this, we can say that the hot electron effect is more prominent in the SC DG transistor. Graded channel DG JLT have less impact of SCE's and hot electron effect as from the simulation we can see that electric field is more at the source side that means it accelerates the electrons in the channel and velocity of the charge carriers increases[14] which causes to increase on- state current.

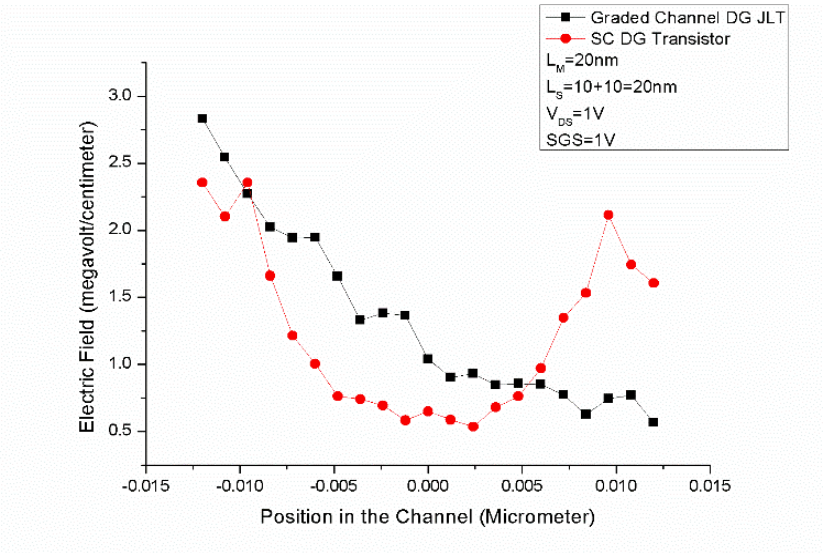

Fig.3. Electric field distribution along the channel.

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Fig. 4 shows the plot of the $I_{DS} - V_{GS}$ curves. The plot is drawn for both Graded channel DG JLT and SC DG transistor at the V_{DS}= 0.05 V and V_{DS} = 1 V at the SGS = 1.5 V and channel length of 30 nm and side gate length 10nm. The graded channel DG JLT have on-state current is 807µA at V_{GS} = 1 V while SC DG transistor have 654µA and off-state current is about $9.10*10^{-14}$ for Graded channel DG JLT and for SC DG transistor it is about $3*10^{-16}$ at V_{GS} = 0V.

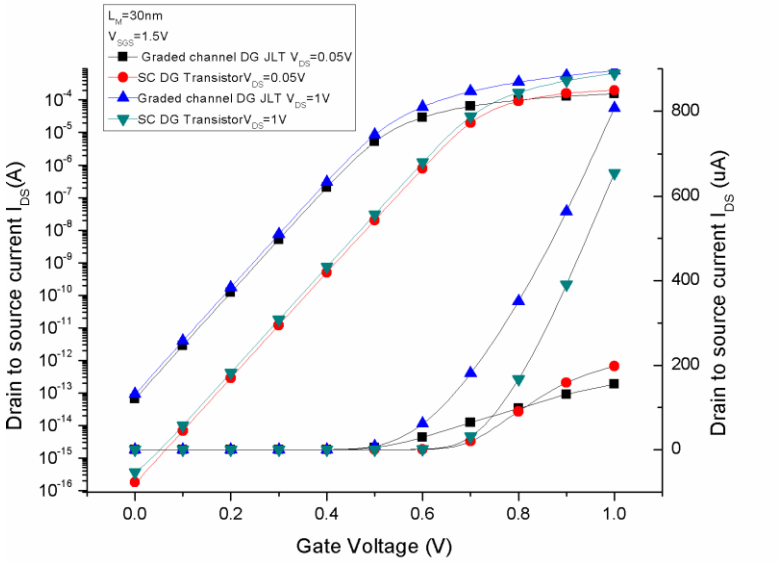

Fig.4. I_{DS}-V_{GS} curves of the n-channel GC DG JLT and SC DG transistor with side gate length = 10 nm and main channel length = 30 nm and V_{SGS} = 1.5V.

On-state current for the Graded channel DG JLT and SC DG transistor for different channel length is shown in the Fig 5. As we increase the channel length from 20 nm to 40 nm we see that on-state current of Graded channel DG JLT is goes on increasing while it goes on decreasing for SC DG transistor. From the figure, we see that current driving ability of the Graded Channel DG JLT is more than that of the SC DG transistor so we can say that S/D series resistance is the minimum in the Graded channel DG JLT compared to SC DG transistor. When the gate voltage is increased the electric field perpendicular to the channel is lower in the JLT which gives advantage in term of drive current to them.

Fig 6 shows the plot of the threshold voltages of the Graded Channel DG JLT and SC DG transistor as a function of channel side gate length at VDS = 1 V, main channel length(LM)
= 20 nm and side gate supply voltage(VSGS) = 1V. The Threshold voltage is calculated by using following equation,

$$I_D = 10^{-7} \times \frac{W}{L} \quad (1)$$

Where W is the width and L is the length of the channel. Threshold voltage variation is largest in the SC DG transistor compared to Graded Channel DG JLT because the threshold voltage of the JLT depends upon the channel depletion. The overlap and under lap issues are absent in the JLT and the effective channel length is more than SC DG transistor.

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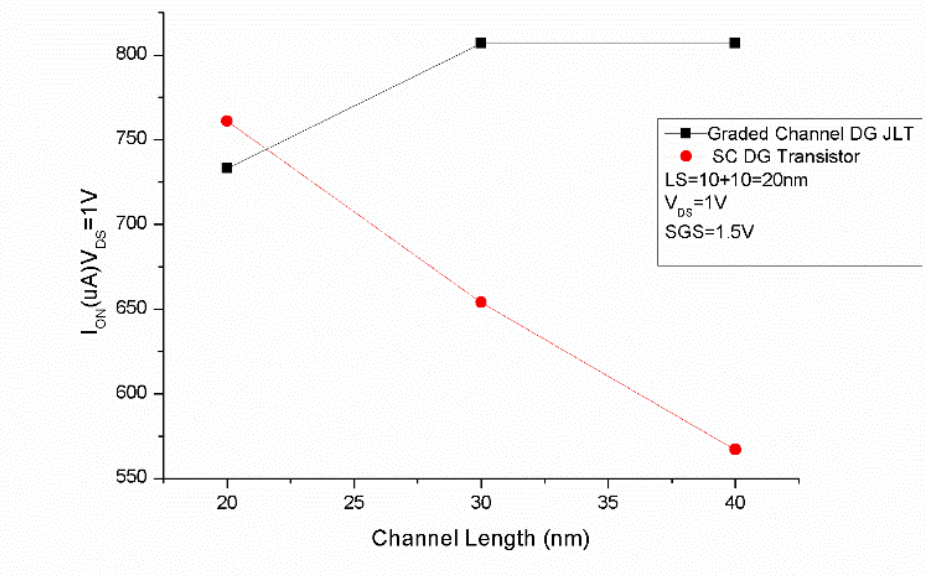

Fig.5. Drive current for GC DG JLT and SC DG transistor with different channel length.

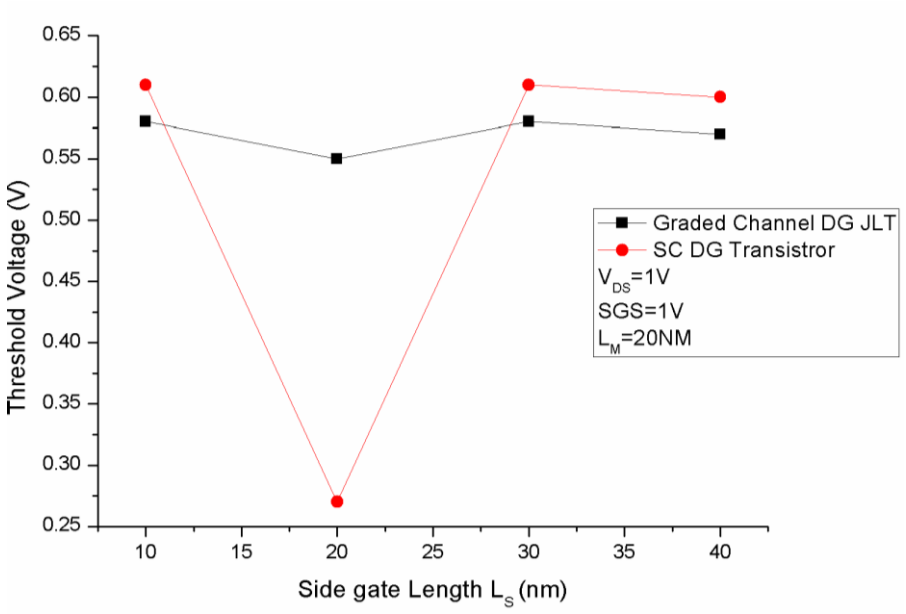

Fig. 6 Threshold voltage of GC DG JLT and SC DG transistor device as a function of channel side gate length

DIBL is demonstrated as difference in threshold voltage for drain bias of 50 mV and 1 V in [19] [20]. DIBL as the function of main channel length is shown in Fig 7. From the Fig.7, we can see that for channel length 20 nm the DIBL is 20 mV and 30 mV for the Graded channel DG JLT and SC DG transistor respectively. We can say that the proposed device has improved DIBL up to 33%.

DIBL as the function of channel side gate length is shown in Fig 8. The Main channel length is 20 nm; side gate supply voltage is 1.5 V and drain bias is 1 V. From the Fig, it is observed that even if the side gate length is increased the DIBL of the Graded channel DG JLT is somewhat constant but for the SC DG transistor, it goes on increasing as side gate increases. DIBL is improved to 50% at the side gate length 20 nm and it is improved to 67% at side gate length 30 nm. From these observations, we can say that threshold voltage variation is largest in SC DG transistor while it is very less in Graded channel DG JLT for the side gate length variation.

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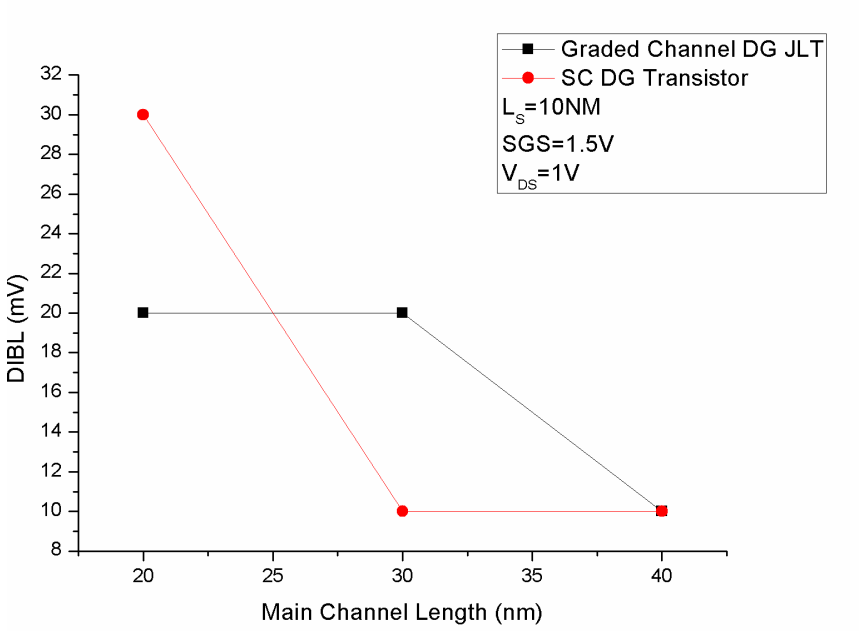

Fig 7. DIBL of GC DG JLT and SC DG transistor as a function of physical gate length.

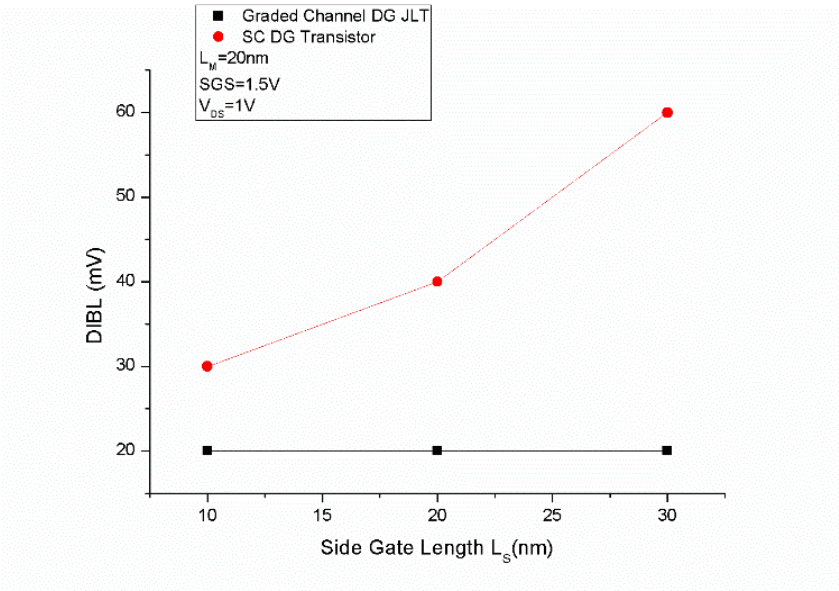

Fig 8. DIBL of GC DG JLT and SC DG transistor as a function channel side gate length.

The plot of the transconductance as a function of the main channel length of Graded channel DG JLT and SC DG transistor at a drain bias of 0.05 V, side gate supply 1.5 V and side gate length 10 nm is shown in Fig 9.a and Fig 9.b respectively. Transconductance is calculated using following formula

$$G_M = \frac{\&I_D}{\&V_{GS}} \qquad (2)$$

From the plot, it is observed that for channel length 20nm transconductance value of the Graded channel DG JLT is 0.15mS and it is 0.05mS for SC DG transistor at gate voltage 0.6V. That is transconductance of Graded channel DG JLT is approximately three times greater than that of SC DG transistor at gate voltage 0.6V.

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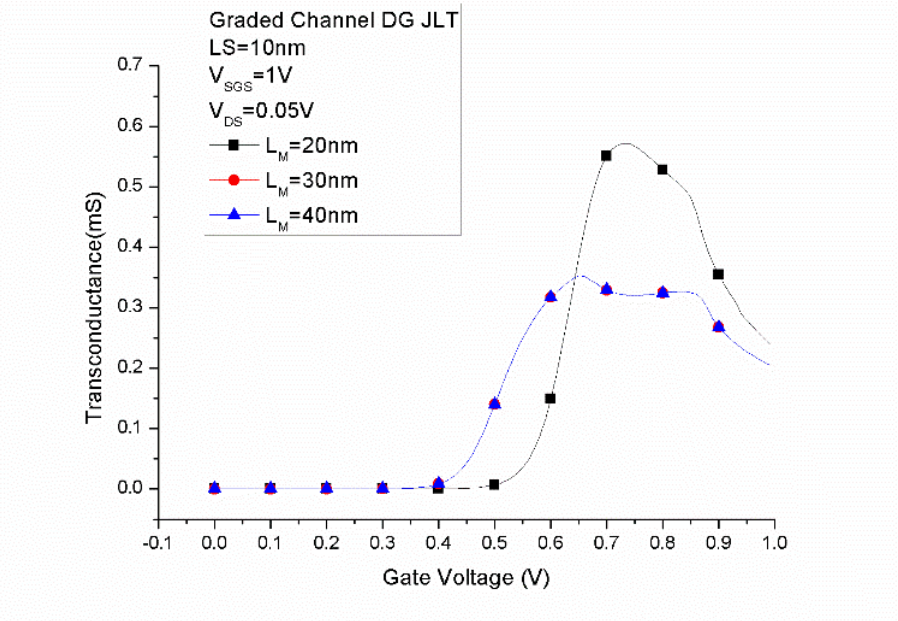

Fig 9.a. Transconductance of GC DG JLT

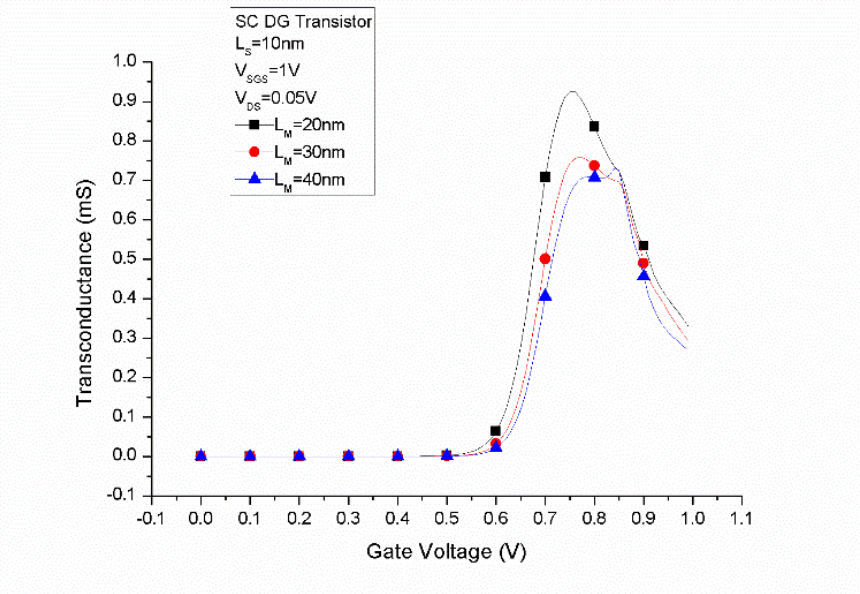

Fig 9.b. Transconductance of SC DG transistor

The Sub-threshold slope as the function of the channel side gate length of the Graded channel DG JLT and SC DG transistor is shown in the following Fig 10. For the calculation of SS following equation is used

$$SS = \frac{d\,V_G}{d(\log(I_D))} \qquad (3)$$

From the plot it is observed that SS of Graded channel DG JLT is better than that of the SC DG transistor. The SS 80 mV/decade is observed for Graded channel DG JLT and 170 mV/decade for SC DG transistor at the main channel length 30 nm, side gate length of 10 nm, side gate supply 1.5 V and drain bias 0.05V. That is SS is improved to 53% in Graded channel DG JLT compared to SC DG transistor.

Fig 11 shows the plot of the Gm/I_{DS}-V_{GS} for both Graded channel DG JLT and SC DG transistor. The ability of the MOSFET to convert DC power into AC frequency and its gain performance is determined from the Gm/I_{DS}

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(21). From the plot, it is seen that Gm/IDS of the Graded channel

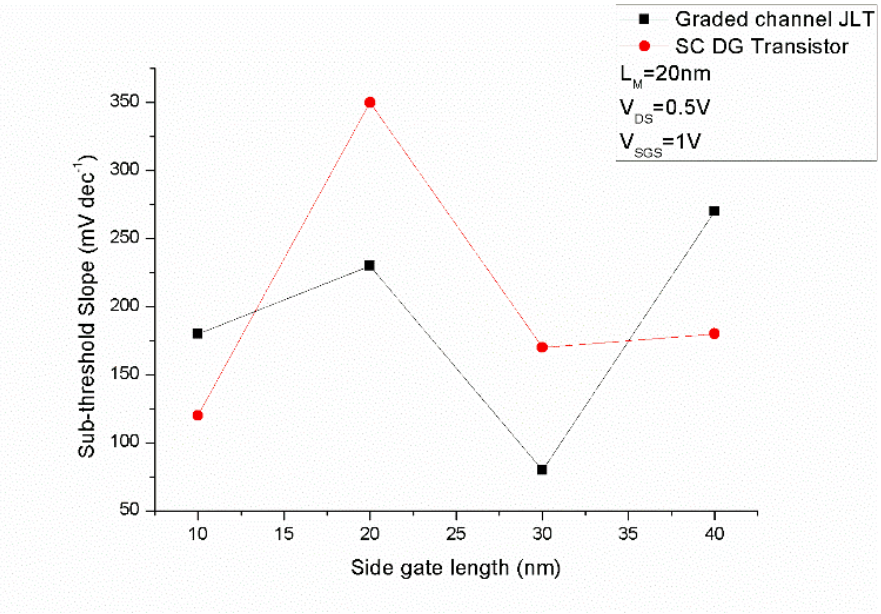

Fig 10. Sub-threshold slope versus main channel side length at VSGS = 1 V.

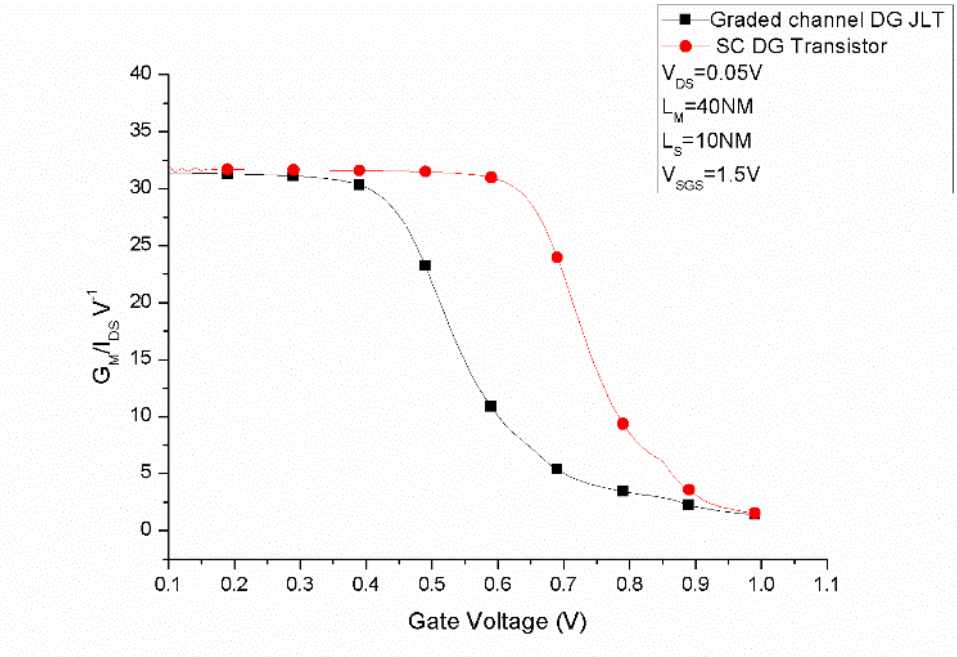

Fig 11. Plots of Gm/IDS as a function of gate voltage for SC DG JLT and SC DG transistor.

DG JLT is the minimum in saturation region compared to SC DG transistor i.e.in the saturation region the drain to source current is maximum for the Graded channel DG JLT, and in the strong/moderate inversion mode it is decreased for Graded channel DG JLT due to lower mobility due to high doping concentration.

III. CONCLUSION

A novel structure GC DG JLT is proposed to reduce the short channel effects for improving the performance of the Junctionless MOSFET in low power and high-performance analog CMOS circuits. The proposed device is simulated using COGENDA TCAD. Results are obtained by varying main channel length from 20 nm to 40 nm as

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well as by varying side gate length along with side gate biasing and are compared with SC DG transistor of equal dimensions. Performance of the nMOS GC DG JL device is evaluated in terms of Vth, DIBL, SS, Gm/IDS, Ion, Ioff, and Gm. It is observed GC DG JLT shows 50% lesser hot electron effect compared to SC DG transistor. At 30 nm channel length and VGS = 1V, the on-state current of GC DG JLT have improved to 19% compared to SC DG transistor. At 40 nm channel length the drive current is improved to 30% in GC DG JLT compared to SC DG transistor. It is also observed that as side gate length is varied from 20 nm to 30 nm; the threshold voltage variation in GC DG JLT is about 3 mv while in SC DG transistor it is 34 mV that is threshold voltage variation is less in GC DG JLT compared to SC DG transistor. At 20 nm channel length DIBL is improved to 33% in GC DG JLT compared to SC DG transistor. Transconductance also three times more in the GC DG JLT than that of SC DG transistor. As the side gate length is varied, the SS is also improved to 53% in GC DG JLT compared to SC DG transistor when the side gate length is 30nm and main gate length is 20 nm. GC DG JLT has a maximum drain to source current in the saturation region. Along with such improved performance together with simple fabrication process, we can remark that Junctionless transistor is strong candidate for future technology nodes.

REFERENCES

[1] Porag jyoti ligira ,Gargi khanna Electronics & Communication Department National Institute of Technology Hamirpur, H.P, India,—Review on different types of Junctionless Transistor, IJETCAS 14- 203; © 2014

[2] Lida Ansari, Baruch Feldman, Giorgos Fagas, Carlos Martinez Lacambra, Michael G. Haverty, Kelin J. Kuhn, Sadasivan Shankar, and James C. Greer, —First Principle-Based Analysis of Single-Walled Carbon Nanotube and Silicon Nanowire Junctionless Transistors, IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 12, NO. 6, NOVEMBER 2013.

[3] Lida Ansari, Baruch Feldman, Giorgos Fagas, Jean-Pierre Colinge, and James C. Greer Tyndall National Institute, University College Cork, Cork, Ireland, —Atomic scale simulation of a junctionless silicon nanowire transistor.

[4] Renan D. Trevisoli, Rodrigo T. Doria, Michelly de Souza, and Marcelo A. Pavanello, Department of Electrical Engineering, —Drain Current and Short Channel Effects Modeling in Junctionless Nanowire Transistors Centro Universitario da FEI, Sao Bernardo do Campo, Brazil.

[5] Tae Kyun Kim, Dong Hyun Kim, Young Gwang Yoon, Jung Min Moon, Byeong Woon Hwang, Dong Moon, Gi Seong Lee, Dong Wook Lee, Dong Eun Yoo, Hae Chul Hwang, Jin Soo Kim, Yang-Kyu Choi, Byung Jin Cho, and Seok-Hee Lee, —First Demonstration of Junctionless Accumulation-Mode Bulk FinFETs With Robust Junction Isolation, IEEE ELECTRON DEVICE LETTERS, VOL. 34, NO. 12, DECEMBER 2013.

[6] Nirmal Ch. Roy, Abhinav Gupta, Sanjeev Rain, —Analytical surface potential modeling and simulation of junction-less double gate (JLDG) MOSFET for ultra-low-power analog/RF circuits, Microelectronics Journal 46 (2015) 916–922.

[7] Seung Min Lee and Jong Tae Park, — The Impact of Substrate Bias on the Steep Subthreshold Slope in Junctionless MuGFETs, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 11, NOVEMBER 2013.

[8] Chi-Woo Lee, Alexei N. Nazarov, Isabelle Ferain, Nima Dehdashti Akhavan, Ran Yan —Low subthreshold slope in junctionless multigate transistors APPLIED PHYSICS LETTERS 96, 102106 (2010).

[9] Thomas Holtij Michael Graef Franziska Hain ,Alexander Kloes Benjamin niguez , —Unified Charge Model for Short-Channel Junctionless Double Gate MOSFETs, MIXDES 2013, 20th International Conference "Mixed Design of Integrated Circuits and Systems" , June 20-22, 2013, Gdynia, Poland.

[10] Chi-Woo Lee, Aryan Afzalian, Nima Dehdashti Akhavan, Ran Yan, Isabelle Ferain, and Jean-Pierre Colinge, —A Junctionless multigate field-effect transistor, APPLIED PHYSICS LETTERS 94, 053511 (2009).

[11] Chi-Woo Lee, Adrien Borne, Isabelle Ferain, Aryan Afzalian, Member, Ran Yan, Nima Dehdashti Akhavan, —High-Temperature Performance of Silicon Junctionless MOSFETs, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 57, NO. 3, MARCH 2010.

[12] Chi-Woo Lee, Isabelle Ferain, Aryan Afzalian, Ran Yan, Nima Dehdashti Akhavan, Pedram Razavi, Jean-Pierre Colinge,—Performance estimation of junctionless multigate transistors, Solid- State Electronics 54 (2010) 97–103.

[13] Debapriya Roy, Abhijit Biswas, —Analytical model of nanoscale junctionless transistors towards controlling of short channel effects through source/drain underlap and channel thickness engineering, Superlattices and Microstructures xxx (2017).

[14] Haijun Lou, Lining Zhang, Yunxi Zhu, Xinnan Lin, Shengqi Yang, Jin He, and Mansun Chan, —A Junctionless Nanowire Transistor With a Dual-Material Gate, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 59, NO. 7, JULY 2012.

[15] S. C. Wagaj, Shailaja Patil & Y. V. Chavan, — Performance analysis of shielded channel double Gate Junctionless and junction MOS transistor International Journal of Electronics Letters, 6:2,192-203,DOI:

DOI: 10.17148/IARJSET.2022.9438

10.1080/21681724.2017.1335785.

[16] Wagaj, S. C., & Chavan, Y. V. (2015). ―Effect of process parameters variation on dual material gate SOI junctionless transistor, IOSR Journal of Electronics and Communication Engineering (IOSRJECE), (2278-2834), 93-99.

[17] Anurag Chaudhry. ―Two-Dimensional Analytical Modeling of Fully Depleted DMG SOI MOSFET and Evidence for Diminished SCEs IEEE Transactions on Electron Devices, VOL.51 No.4, APRIL 2004.

[18] Ali A. Orouji and M. Jagadesh Kumar, ―Shielded Channel Double- Gate MOSFET: A Novel Device for Reliable Nanoscale CMOS Applications, IEEE Trans. On Device And Materials Reliability, Vol. 5, No. 3, September 2005

[19] Chavan, Y. V., & Mishra, D. K. (2008, December 9–10), ―Improved CMOS digital pixel sensor ,Presented at the National Conference on Wireless Communication and Networking organized by L&T, Powai.

[20] Chavan, Y. V., & Mishra, D. K. (2010, December), ―Modeling of the photo-detectors for computer vision system. Published in the International the Journal of Optics by the Springer Publication, 39 (4), 149–156.

[21] Baruah, R., & Paily, R. P. (2014, January). ―A dual-material gate junction less transistor with high-K spacer for enhanced analog performance", IEEE Transaction on Electron Devices, 61(1), 123–128. doi:10.1109/TED.2013.229285.