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Step-up transformer less inverter forpower quality improvement

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Abstract: This work introduces a transformer less inverter topology for power quality improvement. The topology can run on batteries or solar power and has the potential to enhance voltage. This inverter refers to a circuit that converts a DC input into AC without the use of an inductor or a transformer. Inverters without transformers are more compact and lightweight. By utilizing high voltage power electronic switches, this topology's primary goal is to remove inverter losses caused by the use of transformers, which results in a reduction in the inverter system's size, weight, and cost. Energy losses and additional component expenses are avoided using transformer less inverters, making it more cost- effective. A boost converter stage effectively converts a low voltage DC to a high voltage DC, and an H-bridge stage uses the high voltage DC from the boost converter to flip it into a typical 50 Hz AC. The standard two-level inverter topologies and the high gain DC-DC step-up converter are combined into one circuit. The high efficiency DC to DC boost converter is the key reason to eliminate the bulky transformer, it replaces the role of a traditional step-up transformer. The only losses in this system are those produced by the boost converter and H-bridge inverter, which are negligible when compared to the losses from an iron-core transformer. To improve efficiency and lower costs, the trans-former will be removed as part of this project. This article suggests a way for removing power quality problems caused by nonlinear loads, such as sag and swell. Here, power quality problems are minimized by using the inverter's output voltage.

Keywords: DC-DC converter; Two-level inverter; Nonlinear load; step-up transformer less inverter

I. INTRODUCTION

The inverter, which is located in the middle of the solar energy conversion system, trans- forms the direct current (DC) electricity generated by solar panels into alternating current (AC), which is transmitted through the grid. Standard inverters contain a transformer that synchronizes their internal voltage with the grid and appliance voltage. The resulting AC frequency obtained depends on the particular device employed. The power is given by the DC source, not the inverter, which does not generate any energy. Inverters are mostly employed in electrical power applications where significant currents and voltages are present. Rectifiers are electrical circuits that carry out the reverse task, converting AC to DC. Galvanic isolation in grid-connected solar inverters was previously achieved by using transformers between the photovoltaic system and the grid. The transformers used were not only big and heavy, but also difficult to install. They also made the system more complex and were inefficient because of the multiple power stages. Inverters without transformer were introduced in order to address the issues with inverter efficiency, cost, and size. The suggested inverter topology has the potential to increase output AC voltage while converting lower input DC voltage to high AC voltage. By using high voltage power electronic switches, the transformer less inverter's primary goal is to eliminate the losses that occur in the inverter as a result of the presence of a transformer. As a result, the inverter system's size, weight, and price are reduced Power quality problems in electrical systems are exacerbated by non-linear power electronic loads. Increasing non-linear loads have a variety of negative effects on utility supply and power quality issues, such as low system efficiency, poor power factor, derating of power supply equipment, disruption of other customers, interference in adjacent communications networks, etc. Power quality problems including harmonic distortions, overcurrent's, and undercurrents caused by faults and nonlinear loads can be reduced by the suggested inverter topology. It is reduced using the inverter's output voltage. In recent years, solar applications have favored transformer less grid-connected inverters. The conventional two-level inverter setups and the high gain DC-DC step-up converter are combined into one circuit in [1] to form a single- stage inverter configuration.

The suggested inverter topology might increase the AC voltage at the output while also converting the PV module's lower input DC value to a higher AC voltage. Step-up, semi-single stage operation is offered by a transformer less step-up inverter with pulsating DC-link, combined with smaller components. The voltage level is, however, extremely unstable and low in [2]. Paper [3] discusses a transformer-free inverter topology that can address the problems of leakage current and pulsating power in grid-connected photovoltaic (PV) systems at the same time. A family of transformer less inverter topologies with asymmetric phase-legs are validated in [4] and [5]. This study uses a survey of contemporary transformer less inverter topologies and the associated pulse width modulation (PWM) techniques. Using buck and boost operations from dc-link, a common mode transformer less grid feeding topology is depicted in [6]. By Using 5-level Cascaded H-

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bridge Inverter instead of 3-level or 2-level H-bridge Inverter as in [7] and [8] total harmonic distortions present in the output voltage can be minimized. In the example given in [9], an inverter with live switches was used with monopole sinusoidal pulse width modulation (SPWM) and only two switches operating at high frequency. In [10] PV grid-tied applications can adopt H6 transformer less full-bridge inverter topology with low leakage currents are being described, a closed loop has been devised to keep the grid side voltage constant regardless of variations in the input voltage. As a result, switching loss is decreased. The single-phase cascaded transformer less H-bridge PV inverter is examined in reference [11]. The cascaded H4 inverter's common mode leakage current is examined. And it is made clear why the standard cascade H4 inverter is unable to limit leakage current.

One of the crucial concerns for the transformer less PV systems is the reduction of leakage current and is well explained in [12]. In [13], a brand new cascaded H5 inverter is suggested as a potential solution to the leakage current problem. In [14]," a transformer less inverter is demonstrated with an H5 topology. A control loop that can function and keep the output voltage constant despite changes in the load or the environment has been studied. In [15] a single-stage buck-boost inverter with high reliability that may be used as a grid-connected or stand-alone inverter is described. It can produce an output ac voltage that is both higher and lower than the input dc voltage in a single stage. It has the ability to run without PWM dead time and may be used in grid-connected single-phase PV systems without injecting a lot of dc current into the grid. In [16], two set of high voltage gain quasi-switched boost inverters are presented. In [17] Different transformer less inverters that use different methods, such as decoupling the dc from the ac side, clamping the common mode voltage (CMV) during the freewheeling period, or employing common ground designs, are explored in or- der to prevent leakage current. Photovoltaic power using a battery based quasi-Z source cascaded multilevel inverter (BES-qZS-CMI) is discussed in [18]. In [19] a three-phase multilevel quasi-Z-source inverter (qZSI) topology operating in normal and fault-tolerant operation mode is discussed. The structure is composed by two symmetrical quasi-Z-source networks and a three-phase T-type inverter. Besides the intrinsic advantages of multilevel voltage source inverters, the structure is also characterized by their semiconductor fault tolerance capability. In this paper, a transformer less inverter circuit which can boost the output AC voltage and at the same time converts the lower input DC voltage to higher AC voltage are discussed. The output voltage of the inverter can mitigate power quality issues like harmonic distortions, over current and under current due to faults nonlinear loads in a single-phase system.

II. OBJECTIVE

Transformer less inverter's primary goal is to minimize the losses that occur in the inverter as a result of the presence of a transformer. As a result, the inverter system's size, weight, and price are reduced. Objective of this project is to realize a transformer less inverter that can mitigate the power quality issues like sag and swell due to nonlinear loads in a single-phase system by using inverter's output voltage. Also, the aim of this system is to eliminate the losses taking place in inverter due to the presence of transformer by utilizing the high voltage–power electronic switches. This inverter topology has voltage boosting capability. This can also be used to eliminate leakage current.

III. PROPOSED STEP-UP TRANSFORMERLESS INVERTER TOPOLOGY

A. Proposed step-up transformer less inverter topology and operating modes

Transformer less inverters (TL) are becoming more and more common. They convert DC to high frequency AC, back to DC, and then to standard frequency AC using a computerized multi-step process using electronic components. Transformer less inverters are small, lightweight, and reasonably priced. Traditional inverters utilize a single power point, therefore panels operating at low frequencies will reduce the system's overall DC output. There is no electrical separation between the DC and AC circuits in transformer less inverters. Transformer free inverters have been created for Grid-Tie Solar PV Systems; therefore, users of Off-Grid systems may not yet experience the same benefit. An inverter without a transformer is one that satisfies the concept of a transformer less inverter. Transformer less inverters still perform the important task of stepping up the voltage because it is necessary; however, they do so in a completely different way. Figure.1 displays the block schematic of the boost inverter that will be employed in the suggested system. H Bridge inverter, which is made up of four Mosfets, receives power from the dc-to-dc converter's output.

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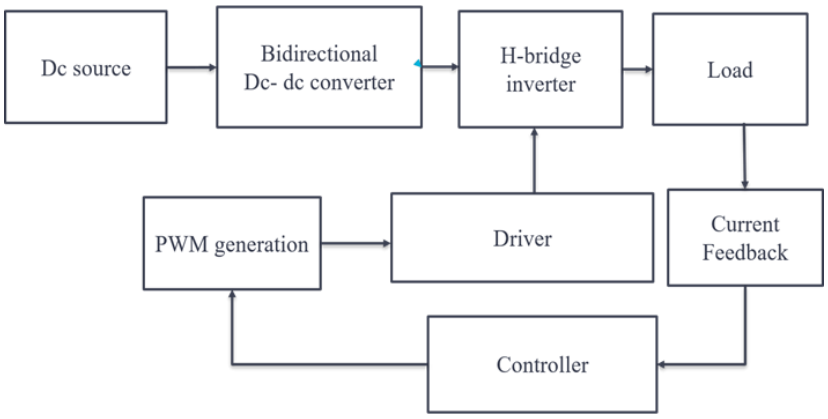

Figure 1: Block diagram of transformer less inverter.

The suggested step-up transformer less inverter topology is depicted in Figure 2. There are six power switches on it (S_1 to S_6), two power diodes D_1, D_2, two high frequency inductors L_1, L_2, and three DC capacitors C_1 to C_3. Among the six power switches, S_1 and S_2 operate at high frequency always (i.e., at switching frequency) while the other four switches S_3 to S_6 either operate at switching of line frequency. The switch pairs (S_1, S_2), (S_3, S_4) and (S_5, S_6) are complimentary. There is thus a total of three distinct gate drive signals needed for the switches in the suggested step-up inverter configuration. Switches are made of MOSFETS. Therefore, a total of three separate gate drive signals is needed for the suggested step-up inverter structure. The suggested inverter topology has four operating modes that correspond to the CCM operation.

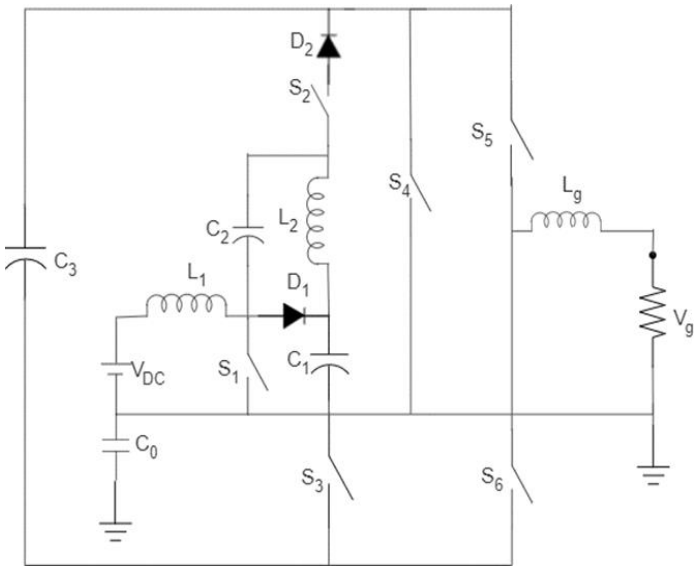

Figure 2: Transformer less inverter circuit.

Table 1: Operating modes

S_1	S_2	S_3	S_4	S_5	S_6	**Modes**
1	0	1	0	1	0	1
0	1	1	0	0	1	2
1	0	0	1	0	1	3
0	1	1	0	0	1	4

Mode 1:(t_0, t_1) It relates to the time during the positive half-cycle when energy is transferred. The power switches S_1, S_3 and S_5 are switched ON during this mode. Energy is stored in the input inductors L_1 and L_2 by the input source and auxiliary capacitor (C_1. As a result, the linear growth of the inductor currents i_{L1} and i_{L2} is observed. Following are the equations for the currents i_{L1} and i_{L2} and voltages across L_1 and L_2 that correspond to this mode:

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$$V_{L1} = V_{DC}$$

$$V_{L2} = V_{C1} - V_{C2}$$

$$i_{L1}(t) = \frac{V_{DC}}{L_1}(t - t_0) + i_{L1}(t_0)$$

$$i_{L2}(t) = \frac{V_{C1} - V_{C2}}{L_2}(t - t_0) + i_{L2}(t_0)$$

Mode 2:(t_1, t_2) It relates to the time when the engine is free to move during the positive half-cycle. In this mode, the load acts as a conduit for current flowing freely through the switches S_3 and S_6 in the inductor L_g. Additionally, during mode 1, the energy stored in the inductors is transferred to the capacitors C_1 and C_3. Following are the voltages across L_1 and L_2 that correspond to this mode:

$$V_{L1} = V_{DC} - V_{C1}$$

$$V_{L2} = -V_{C2}$$

$$i_{L1}(t) = \frac{V_{DC} - V_{C1}}{L_1}(t - t_1) + i_{L1}(t_1)$$

$$i_{L2}(t) = \frac{-V_{C2}}{L_2}(t - t_1) + i_{L2}(t_1)$$

Mode 3:(t_3, t_4) It is equivalent to the time when energy is transferred during the negative half-cycle. The power switches S_1, $S_4$and S_6 are switched ON while the device is in this mode. Similar to mode 1, this mode also stores energy in the input inductors L 1 and L 2 via the V_{DC} input source and V_{C1} auxiliary capacitor, respectively. The following are the inductor currents i_{L1} and i_{L2} that correspond to this mode:

$$V_{L1} = V_{DC}$$

$$V_{L2} = V_{C1} - V_{C2}$$

$$i_{L1}(t) = \frac{V_{DC}}{L_1}(t - t_3) + i_{L1}(t_3)$$

$$i_{L2}(t) = \frac{V_{C1} - V_{C2}}{L_2}(t - t_3) + i_{L2}(t_3)$$

Mode 4:(t_4, t_5) The freewheeling phase of the negative half-cycle is where it falls. The freewheeling time of the inverter for the negative half cycle of the load voltage is covered in Mode 4. Similar to mode 2, the inductor current L_g in this mode likewise freely oscillates through the switches S_3 and S_6 via the load. Additionally, in this mode, the energy that was previously stored in the inductors during mode-3 is transferred to the capacitors C_1 and C_3. As a result, the currents (i_{L1} and i_{L2} decline linearly. Figure 5.2 displays the present conducting routes in this mode of operation. The voltages across L_1 and L_2 that correspond to this mode are as follows:

$$V_{L1} = V_{DC} - V_{C1}$$

$$V_{L2} = -V_{C2}$$

$$i_{L1}(t) = \frac{V_{DC} - V_{C1}}{L_1}(t - t_4) + i_{L1}(t_4)$$

$$i_{L2}(t) = \frac{-V_{C2}}{L_2}(t - t_4) + i_{L2}(t_4)$$

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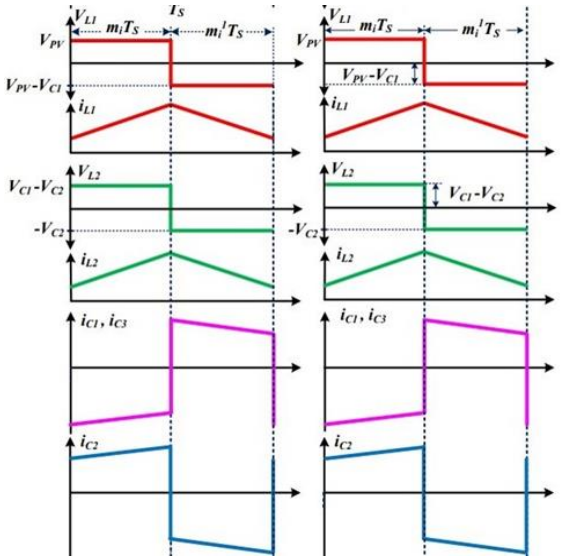

Figure 3: Waveforms of step-up inverter at CCM

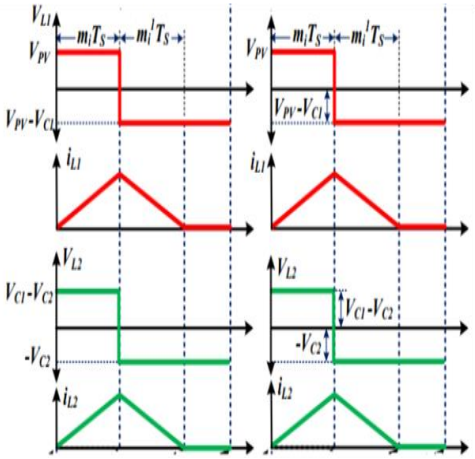

Figure 4: Waveforms of step-up inverter at DCM.

Figure 3 and 4 show the waveforms related to CCM and DCM operation, respectively. There are six different operating modes for the DCM. Figure 3 illustrates the DCM functioning of the proposed inverter architecture and the related powering and freewheeling modes (i.e., modes 1 to 5). It also depicts the current-conducting channels for the DCM operation's mode- 3 [t_2, t_3], and mode-6 [t_6, t_7]. Due to the complete de-energization of the inductors L_1 and L_2, the current in both of them is zero during these modes. Through switches S_3 and S_6, the inductor L_g stored energy continues to supply the load. For modes 3 and 6, the currents through L_1 and L_2 are reported as follows:

B. Design Parameters of the Proposed topology

By taking average of voltage over a switching cycle across the inductor L,

$$\int_0^{m_{iTS}} V_{DC}\,dt + \int_{m_{iTS}}^{T_S} V_{DC}\,dt = 0$$

$$\int_0^{m_{iTS}} (V_{C1} - V_{C2})\,dt + \int_{m_{iTS}}^{T_S} -V_{C2}\,dt = 0$$

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$$V_{C3} = V_{C2} + V_{C1},$$

$$V_{C1} = \frac{V_{DC}}{1 - m_i}$$

$$V_{C2} = \frac{m_i}{1 - m_i} V_{DC}$$

$$V_{C3} = \frac{1 + m_i}{1 - m_i} V_{DC}$$

$$V_0 = m_i V_{C3}$$

$$Gain, G = \frac{V_0}{V_{DC}} = \frac{1 + m_i}{1 - m_i} m_i$$

Based on the voltage across and current passing through them, respectively, inductors and capacitors are designed. Calculating average current in the inductors is required for that. When charging, the inductor current is given as,

$$(i_{L1})_a vg = \frac{1}{2} \Delta i_{L1}$$

$$(i_{L2})_a vg = \frac{1}{2} \Delta i_{L2}$$

for a lossless system,

$$P_i = P_0$$

$$V_{DC} \times i_{DC} = P_0$$

Now critical inductance required for L_{1C} and L_{2C} is found as,

$$L_{1C} = \frac{m_i \times V_{DC}^2}{2 P_0 f_s}$$

$$L_{2C} = \frac{m_i \times (V_{C1} \times V_{C2})^2}{2 P_0 f_s}$$

For capacitor design, assuming voltage ripple of 5%

$$C_1 = C_2 = C_3 = \frac{P_0}{\Delta V_{C1,2,3} \times V_{C1,2,3} \times f_s}$$

IV. PULSE WIDTH MODULATION AND CONTROL TECHNIQUES OF THE STEP-UP INVERTER TOPOLOGY

In the Proposed System PWM is a modulation method that creates pulses with changing widths to simulate the amplitude of an analogue input signal. In this PWM method, gate pulses are generated for all controllable switches by com- paring the modulating wave Vmsin(wt) with a repeating waveform (Vtri). To create the necessary gate pulses, logic operations must be applied to the signals acquired from the above comparison. Figure 6 depicts a logic diagram. The created PWM method for the suggested inverter topology is shown in Figure 5. The gate pulses S_1 and S_2 may be shown to operate at

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switching frequency for a whole sinewave cycle. S_3 and S4 operate at both line frequency and switching frequency in the positive and negative half cycles respectively. The S_5 and S_6 operate similarly at line frequency and switching frequency.

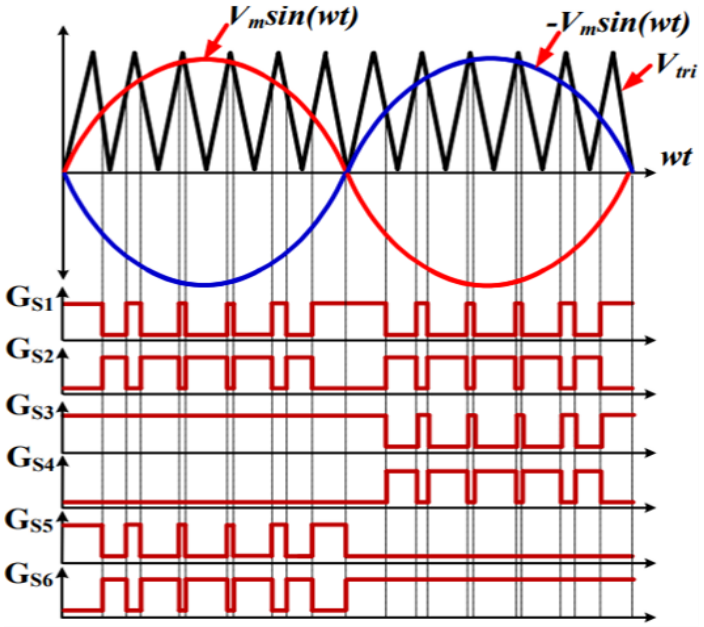

Figure 5: Developed PWM technique of the proposed step-up inverter.

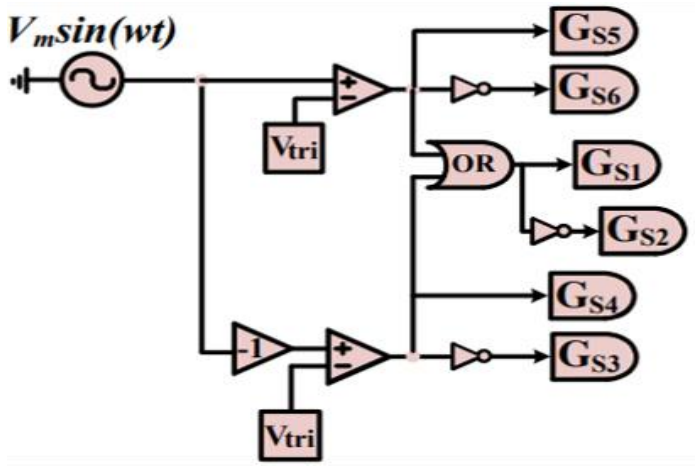

Figure 6: Modulation logic diagram for the developed PWM technique.

V. SIMULATION AND EXPERIMENTAL RESULTS OF THE STEP-UP INVERTER TOPOLOGY

The proposed inverter is simulated in MATLAB and the results are studied to confirm the analytical behavior in order to assess the inverter performance and the theoretical calculations. A DC supply of 8 to 10 V is applied at the input which has been boosted at a duty ratio of 0.6 giving an output of 28 to 40 V. Using MATLAB/SIMULINK, simulation studies are carried out to assess the performance of the proposed DC-DC Converter. Table 6.1 below lists the circuit parameters used in the simulation analysis.

Table 2: Simulation parameters

PARAMETERS	VALUES
f_s	20 kHZ
V_{in}	10 V
D	0.6
L_1, L_2	350 µH

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L_g	2 mH
C_3	180 µF
C_1, C_2	47 µF
C_3	0.1 µF

Figure 7 shows the complete simulation diagram of the proposed inverter circuit. That is inverter circuit along with its control and a circuit with nonlinear loads and fault are illustrated. The transformer less inverter output is given to the nonlinear circuit and corresponding control signals for the inverter circuit is implemented. The gate drive circuit of switches receives the control signal. As a voltage-driven device, the MOSFET has no DC current flowing into the gate. A voltage that is greater than the rated gate threshold voltage must be delivered to the gate in order to switch on a MOSFET. The PWM generator receives feedback signals from the control circuit. The entire system is appropriate for both linear and non-linear output loads. PWM is a frequently used control method that converts digital signals from electronics like microcontrollers into analogue signals.

A. Simulation results

The input voltage waveform is shown in figure 7. It shows the operation waveforms for the inverter while operating in CCM. The output voltage and current waveforms of the model is shown in figure 8. Input voltage is 10 V and output voltage obtained is around 40 V.

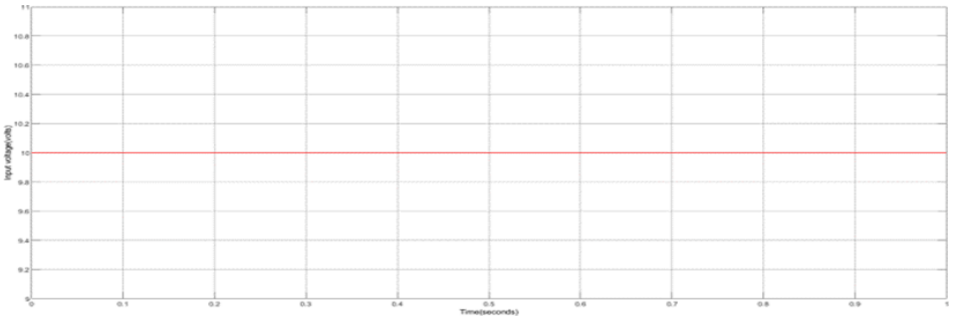

Figure 7: Voltage at input side versus time in sec.

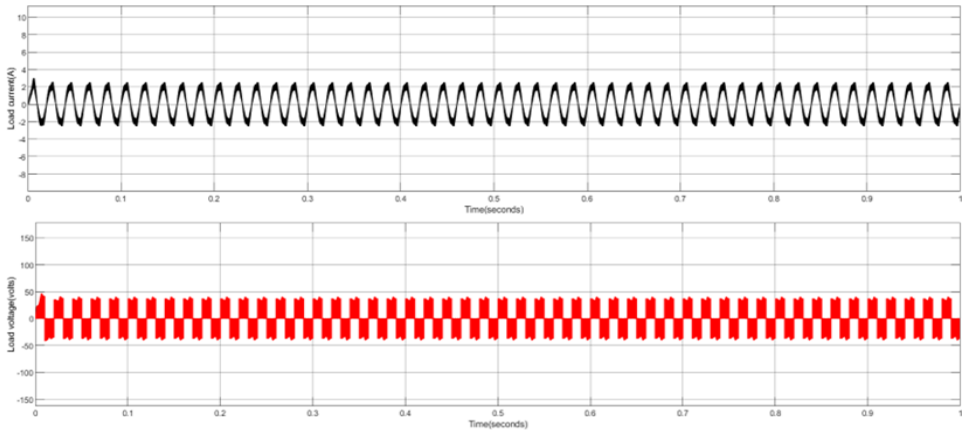

Figure 8: Voltage at output side versus time in sec.

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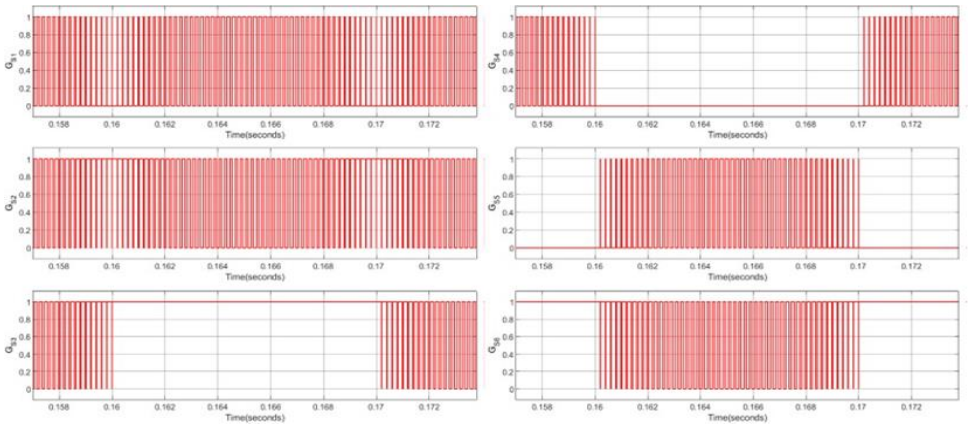


Figure 9: Developed PWM waveforms.

Figure 9 shows the simulation output of the generated PWM. In this modulation technique the modulating wave Vmsin(wt) is compared with a repeating waveform (Vtri)to produce gate pulses to all controllable switches. The carrier wave usually has a much higher frequency than the modulating wave. The triangular waveform is the most commonly used. It could be observed from figure 10, that both the input inductors L_1 and L_2 are operating in CCM. The inductor current in the energy transfer period never approaches zero value while in continuous conduction mode inductor current approaches zero. The inductors current pattern is natural by way of being magnetized while switches are ON and demagnetize if switches are turned OFF. The current flows steadily from the higher terminal of the inductor to the lower terminal of the inductor while the switch is closed. In steady state, there is extremely little overshoot and very little ripple in the inductor current. Figure 6.8 and 6.9 shows the waveforms of the voltage across auxiliary capacitors V_{C1}, V_{C2}, V_{C3} and V_{C0}.

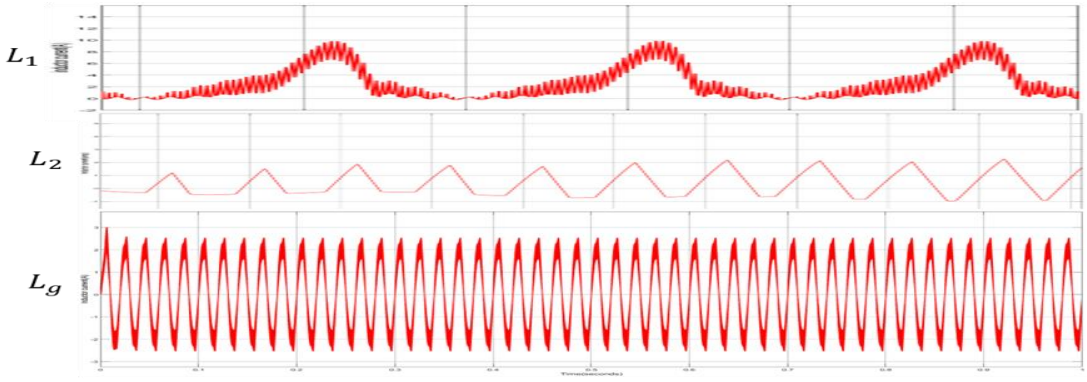
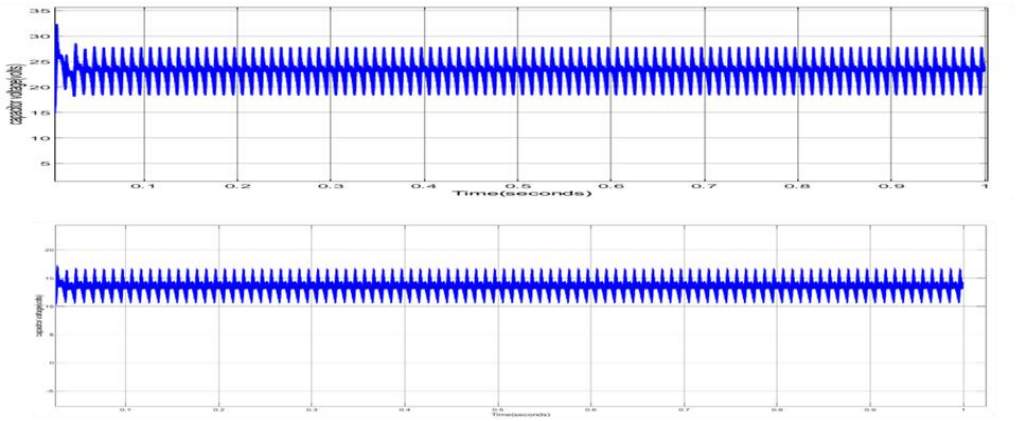


Figure 10: Current through inductors versus time in sec.



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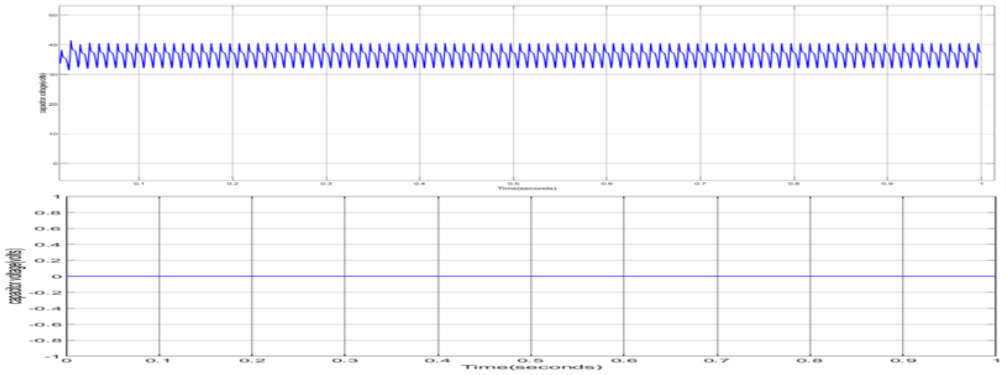

Figure 11: Voltage across capacitors versus time in sec.

Figure 12 shows the nonlinear load current waveforms and figure 13 shows the nonlinear load voltage waveforms. The nonlinearity can be observed from the waveforms. Non-linear loads can cause the production of frequency component of the currents in the system which is not fundamental frequency components. So due to such harmonic component of currents the quality of power gets affected and causes many issues like sag and swell. Power quality issues in source current due to non-linear loads and fault in the circuit are shown in figure 14. From figure14 it is clear that there are power quality issues like sag and swell in the source current. By applying the output voltage of the proposed transformer less inverter to the circuit where nonlinear loads are attached, selective harmonic and power quality issues can be avoided.

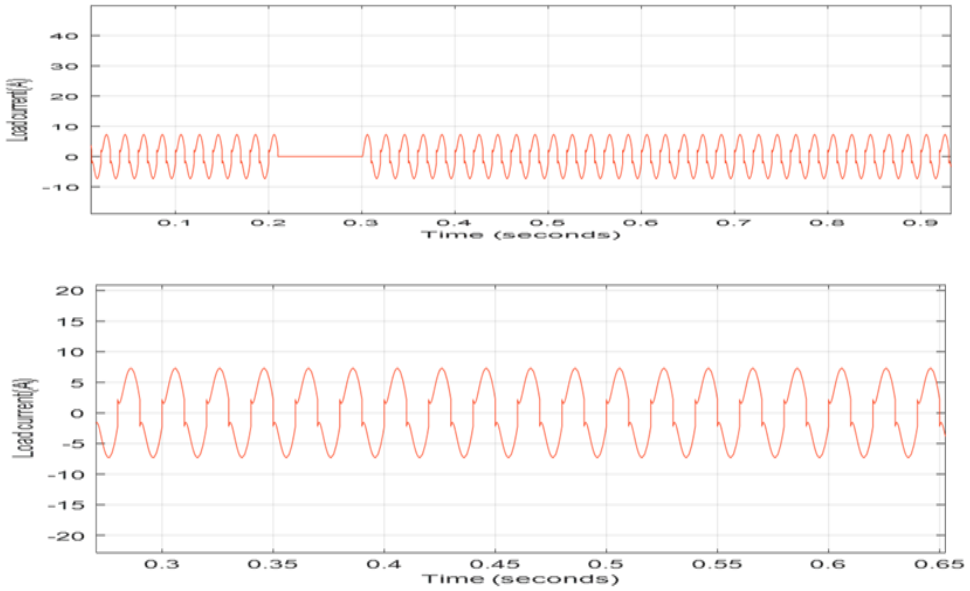

Figure 12: load current waveforms

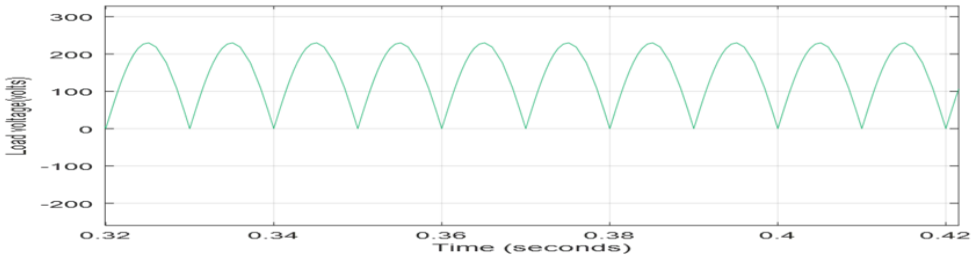

Figure 13: load voltage waveform

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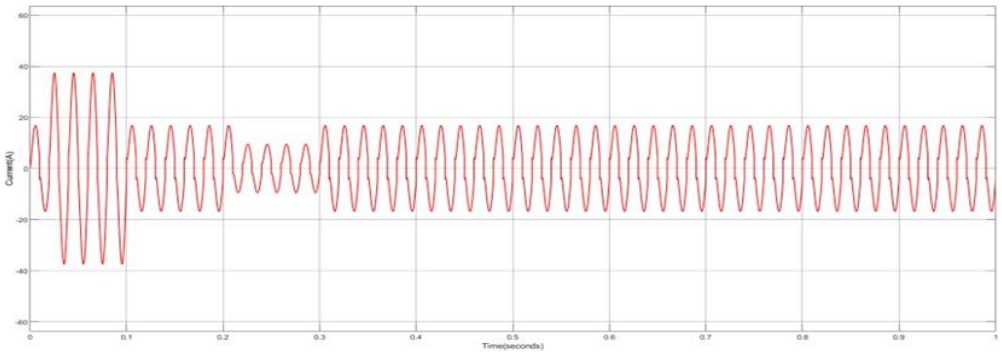

Figure 14: Source current waveform

Power quality problems including harmonic distortions, overcurrent's, and undercurrents caused by faults and nonlinear loads can be reduced by the suggested inverter topology. It is reduced using the inverter's output voltage Power quality problems including harmonic distortions, overcurrent's, and undercurrents caused by faults and nonlinear loads can be reduced by the suggested inverter topology as shown in figure 15. It is reduced using the inverter's output voltage can be added in this system easily, the system is flexible and technically feasible. The system can be improved according to the need in future.

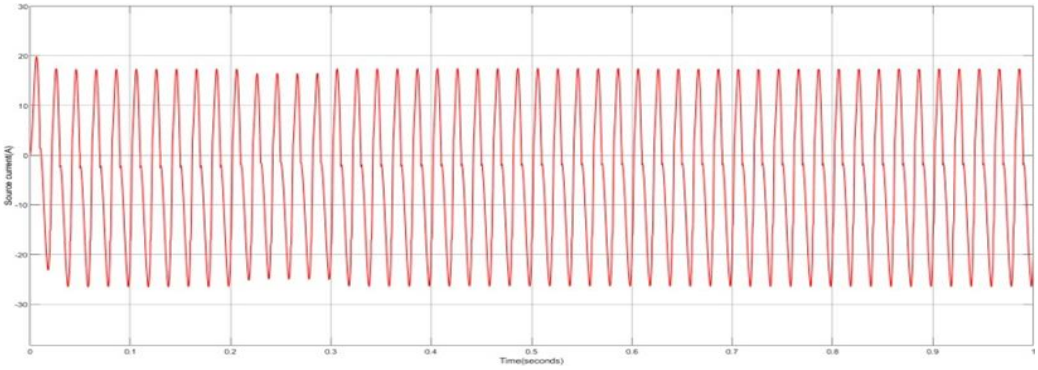

Figure 15: Source current waveform

A. Experimental results

An experimental prototype has been constructed to verify the feasibilities of the proposed inverter by using the design parameters. Parameters for the hardware prototype are shown in Table.

Table 7.1: Hardware parameters

Parameters	Values
Input voltage/Output voltage	8-10V/28-30V
Switching frequency	20 kHZ
Duty ratio	0.6
Inductors	L_1=10 A 350 µH, L_2=5A 350 µH, Lg=2 mH
Capacitors	C_1=C_2=47 µF, 47 µF, C_3=180 µF, C_0 = 0.1 µF
MOSFET	1RFB4110,1RFP240
Diodes	MUR1560
Optocoupler	TLP250

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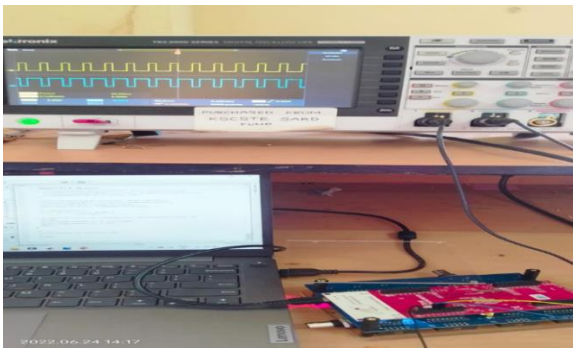


Figure 16: PWM Generator

The complete hardware setup of the inverter circuit is shown in figure 17. The Input is varied from 8Vto 10V which produces a boosted inverted. Output of 28 to 30V.Output square wave is generated. Figure 18 shows the PWM generated using DSP. In this modulation technique the modulating wave Vmsin(wt) is compared with a repeating waveform (Vtri)to produce gate pulses to all controllable switches. Switches (S_1, S_2), (S_3, S_4), and (S_5, S_6) are complementary switch pairs

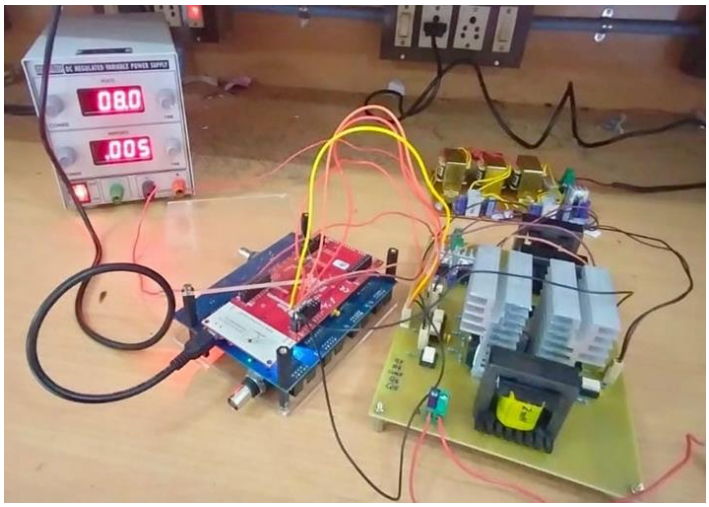
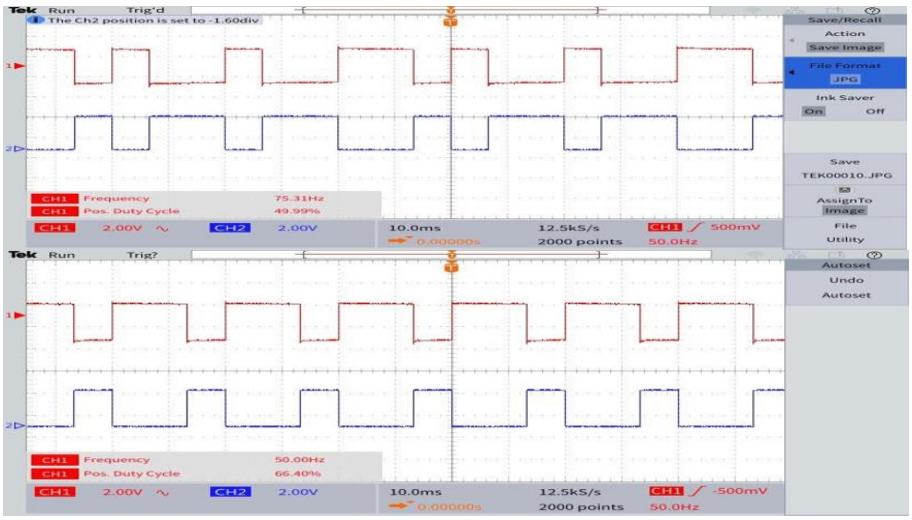


Figure 17: Inverter prototype.



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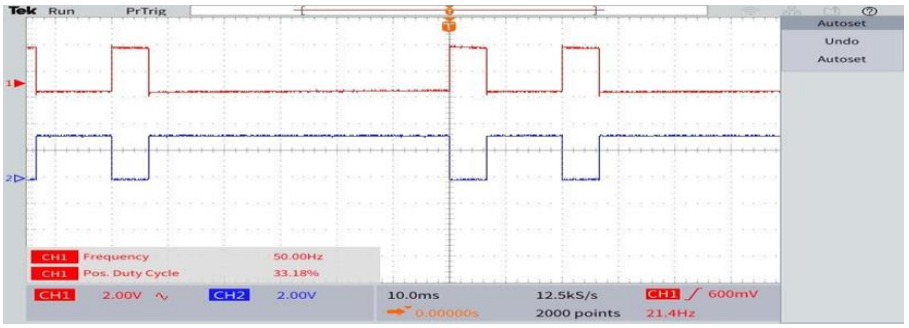
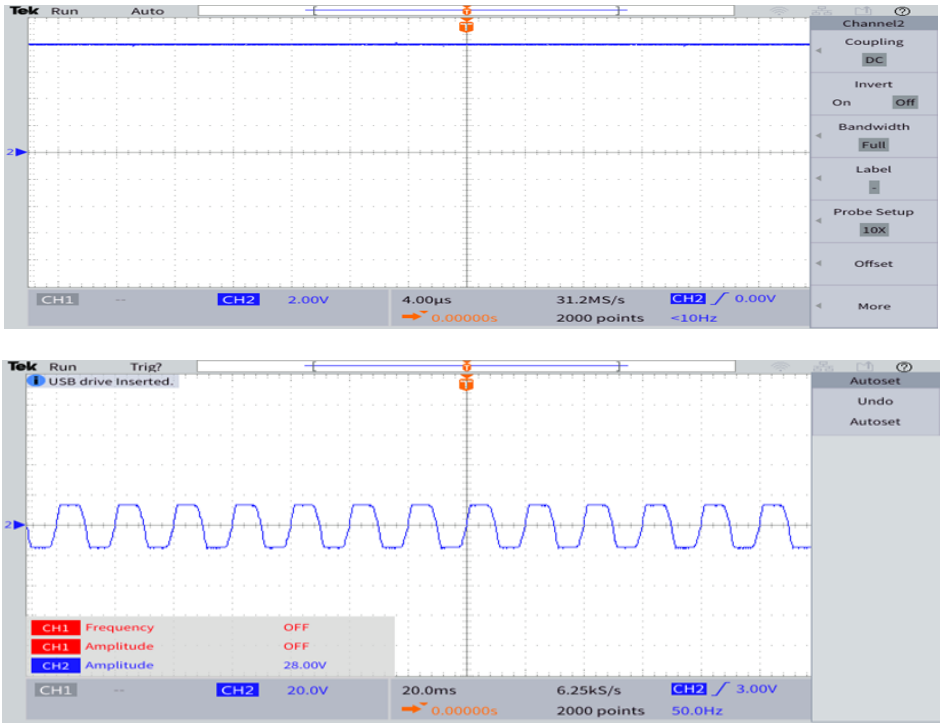


Figure 18: Developed PWM for (S_1, S_2), (S_3, S_4), and (S_5, S_6)

The input and output voltage waveform of the proposed inverter is shown in figure 19. For an input voltage of 8V inverter produced 28V at the output.



It is obvious that the supplied input DC voltage has been transformed into enhanced AC voltage. While also converting the lower input DC voltage to AC voltage, the suggested inverter structure could increase the output AC voltage. Last but not least, the experimental analysis of the suggested step-up inverter shows that it can increase the lower input DC voltage by 2 to 4 times. As a result, the experimental findings support the findings of the analysis and simulation,

VII. FUTURE SCOPE

According to the direction of research, solar cell prices should decrease in the future. The distribution generation system for renewable energy can use the inverter design under discussion. This architecture can make the equipment smaller, making it more portable and able to fit in smaller spaces. By utilizing the appropriate switching circuits and inductor coils, the design can be expanded.

VII. CONCLUSION

Single-phase transformer less PV inverters have attracted a lot of attention due to their low cost, weight and high efficiency compared to single-phase inverters with galvanic isolation. In this study, a step-up transformer less inverter architecture is proposed that reduces or completely gets rid of leakage currents. The creation of lossless inverters is the

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project's principal objective. As a result, the transformer was removed from the circuit and replaced with other components that may provide greater efficiency than a typical transformer inverter. The suggested one-stage inverter topology fuses the conventional two-level inverter configuration and the high gain DC-DC step-up converter into a single circuit. The proposed inverter topology could thereby increase the output AC voltage. The proposed inverter topology's laboratory tests employing a TMS320F28379D DSP controller produced positive results. The only losses in this system are those produced by the boost converter and H-bridge inverter, which are negligible when compared to the losses from an iron-core transformer. Transformer-based inverters are more expensive than transformer-less inverters because they need additional components, which add to the cost. Power quality problems in the electrical system are exacerbated by non-linear power electronic loads. The suggested inverter topology can reduce problems with power quality such harmonic distortions, over- currents, and undercurrents caused by nonlinear faults. The proposed step-up inverter's experimental study has shown that it can increase the lower input DC voltage. To lessen harmonics, an inverter's output voltage is employed. To ensure that the suggested topology simulations are run in MATLAB and that the simulation results are closely related with the theoretical analysis.

REFERENCES

[1] P. K. Chamarthi, M. S. El Moursi, V. Khadkikar, K. H. A. Hosani, and T. H. M. El-Fouly, "Novel step-up transformerless inverter topology for single phase grid-connected photovoltaic system," IEEE Transactions on Industry Applications, vol. 57, no. 3, pp. 2801–2815, 2021.

[2] S. M. Babu, B. L. Narasimharaju, and A. K. Rathore, "A new pulsating dc-link three-phase transformerless inverter for renewable applications," pp. 1–4, 2020.

[3] B. Chen and J.-S. Lai, "A family of single-phase transformerless inverters with asym- metric phase-legs," pp. 2200–2205, 2015.

[4] Y. R. Kafle, G. E. Town, X. Guochun, and S. Gautam, "Performance comparison of single-phase transformerless pv inverter systems," pp. 3589–3593, 2017.

[5] K. H. Nanwani and D. S. More, "A buck-boost common-mode transformerless inverter for photovoltaic applications," pp. 1–5, 2018.

[6] E. E. Ahsan, M. A. Shobug, M. M. H. Tanim, and M. H. Reza, "Harmonic distor- tion reduction of transformerless inverter's output voltage using 5-level single-phase inverter and lcl filter," pp. 251–256, 2020.

[7] B. Karur and S. R A, "Multi-level transformerless pv inverter based real and reactive power injection for single phase system," pp. 258–262, 2020.

[8] A. Das and G. Sheeja, "Photovoltaic h6-type transformerless inverter topology," pp. 1–5, 2017.

[9] Z. Yu, X. Hu, Z. Yao, L. Chen, M. Zhang, and S. Jiang, "Analysis and design of a transformerless boost inverter for stand-alone photovoltaic generation systems," CPSS Transactions on Power Electronics and Applications, vol. 4, no. 4, pp. 310– 319, 2019.

[10] Q. Huang, A. Q. Huang, R. Yu, P. Liu, and W. Yu, "High-efficiency and high-density single-phase dual-mode cascaded buck–boost multilevel transformerless pv inverter with gan ac switches," IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7474–7488, 2019.

[11] H. Li, Y. Zeng, B. Zhang, T. Q. Zheng, R. Hao, and Z. Yang, "An improved h5 topol- ogy with low common-mode current for transformerless pv grid-connected inverter," IEEE Transactions on Power Electronics, vol. 34, no. 2, pp. 1254–1265, 2019.

[12] X. Guo, X. Jia, Z. Lu, and J. M. Guerrero, "Single phase cascaded h5 inverter with leakage current elimination for transformerless photovoltaic system," pp. 398–401, 2016.

[13] M. A. Khan, A. Haque, and K. Bharath, "Control and stability analysis of h5 trans- formerless inverter topology," pp. 310–315, 2018.

[14] A. A. Khan, H. Cha, U. A. Khan, and H.-G. Kim, "Four-switch buck-boost inverter for stand-alone and grid-connected single-phase pv systems," pp. 460–465, 2017.

[15] M.-K. Nguyen, T.-D. Duong, Y.-C. Lim, and J.-H. Choi, "High voltage gain quasi- switched boost inverters with low input current ripple," IEEE Transactions on In- dustrial Informatics, vol. 15, no. 9, pp. 4857–4866, 2019.

[16] J. Wang, B. Ji, J. Zhao, and J. Yu, "From h4, h5 to h6 —standardization of full- bridge single phase photovoltaic inverter topologies without ground leakage current issue," pp. 2419–2425, 2012.

[17] W. Liang, H. Abu-Rub, Y. Liu, and B. Ge, "State-of-charge balancing control for battery energy stored quasi-z source cascaded multilevel inverter based photovoltaic power system," pp. 8–13, 2015.

[18] V. Fernão Pires, A. Cordeiro, D. Foito, and J. F. Martins, "Quasi-z-source inverter with a t-type converter in normal and failure mode," IEEE Transactions on Power Electronics, vol. 31, no. 11, pp. 7462–7470, 2016.

[19] Y. Tang, W. Yao, P. C. Loh, and F. Blaabjerg, "Highly reliable transformerless photovoltaic inverters with leakage current and pulsating power elimination," IEEE Transactions on Industrial Electronics, vol. 63, no. 2, pp. 1016–1026, 2016.

