IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified ⁜ Impact Factor 7.105 ⁜ Vol. 9, Issue 8, August 2022

DOI: 10.17148/IARJSET.2022.9823

DESIGN OF DUAL EDGE TRIGGERED SEQUENTIAL CIRCUITS USING QUANTUM DOT CELLULAR AUTOMATA

Jameel Ahmed Kustagi[1], Dr.Abhishek M.B[2]

M.Tech Student, ECE Department, Dayananda Sagar College of Engineering, Bengaluru, Karnataka, India[1]

Asst. Professor, ECE Department, Dayananda Sagar College of Engineering, Bengaluru, Karnataka, India[2]

Abstract: The cellular automaton with quantum dots, is a branch of nanotechnology, can be used to create combinational and sequential circuits at the nanoscale, by manipulating the position of the electron. In comparison to existing transistor-based SR, JK T, and D flip-flops, QCA technology offers a number of additional benefits, including low power consumption, faster speed, small size, and great performance. When compared to a single edge triggered QCA circuit, the dual edge triggered QCA structure offers minimal power consumption and fast switching. The primary design criteria for circuits include cell count, and area usage, [9] to compare the two edges triggered flip-flops with the one edge-triggered flip-flops, and we create both types of flip-flops in this work.

Keywords: QCA, Majority gate, Dual edge flip flop, single edge flip flop

I. INTRODUCTION

QCA emerged as a popular technology for designing micro and Nano-scale electronic devices. In designing digital circuits, the position of a single electron is crucial and can take the place of CMOS technology [1]. QCA structure overcomes the shortcomings of CMOS design, such as scale, switching activity, area, and speed [2]. The QCA technology will be used in the construction of wireless digital circuits. High switching speed, high density, and incredibly low power input can all be achieved using QCA. A bi-stable cell comprised a set of four quantum dots powered by free electrons is the basis for the QCA technology. The QCA technology works well for applications requiring extremely weak power, highly dense, and functioning at THz frequencies, where QCA cells can be replaced by standard CMOS devices.

Recently, additional circuits were built utilizing QCA, the JK FF, D FF and T FF, as well as the RS flip flop, have been designed and implemented. The D FF was proposed in the study employing two low latency edge-triggered FFs with independent input clocks. In this study, the flip-flops based on DET and SET flip-flops are built using various QCA properties. The QCA designer tool is then used to analyse the design. In this essay, we've covered the crucial background information on the QCA concept that is necessary for creating digital circuits with the QCA technology as well as designing sophisticated DET-FF. Then the designed QCA FF circuits are analyzed and shown with the difference between the single edge trigger and dual edge trigger in the section of the paper, the dual edge trigger flip-flop is then used to compare with the single edge trigger QCA technology and at last, conclusion is provided and future scope also provided.

II. QCA BASICS

The sequential circuits such as counters, registers and memories are commonly designed using logic gates and CMOS technology. The binary data is saved in a QCA cell in the QCA circuit, hence this technology might be replaced with QCA technology. It is consist of two charged electrons with a negative charge and four quantum dot cells. At the structure's corners are where the quantum dots are situated and the movable electrons occupy the transverse position in the structure. The electrostatic repulsion force between the electrons is the reason electron occupy nearby cell in the QCA circuit. Due to this movement the possible P=-1 and P=+1 polarizations take place, which represents logic 0 and logic 1. This shown in fig.1.The standard QCA cell distance is 20 nm and the standard QCA cell dimensions are 18 nm x 18 nm.

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified ⁜ Impact Factor 7.105 ⁜ Vol. 9, Issue 8, August 2022

DOI: 10.17148/IARJSET.2022.9823

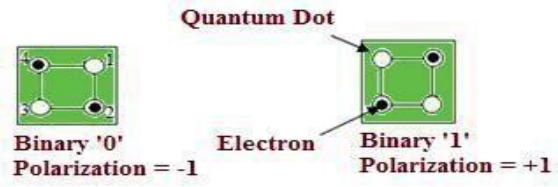


Fig 1. Cells polarizations

The QCA cell, which has one quantum dot in each of its four corners, is the key component that makes up QCA technology. Through electron tunnel junctions, these quantum dots are linked. The QCA cell is 18 nm by 18 nm in dimension and has a square shape. And a 5 nm-diameter a quantum dot is an electron-only storage device, as shown in the Figure. 2. a and 2.b. Depicts the QCA cell in an un-polarized state. The two polarizations, P +1 and P- 1, are present in the cell, based on how the electrons are positioned, as illustrated in Fig. 2c.

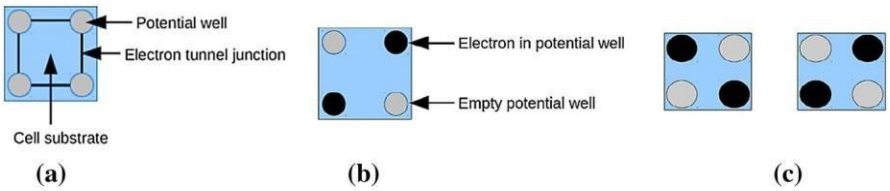


Fig.2. a) QCA cell physiology b) elements of a potential well c) polarization of cell =− 1

Due to the columbic repulsion force between them, every QCA cell contains 2 electrons that were arranged in 2 quantum dots so that they consistently select the quantum dots at the corners of the cell as their location maintaining the biggest space conceivable between them. However, between cells, the two electrons cannot mechanically quantum tunnel.

A. QCA WIRING

A wire is a key component of the QCA structure. Columbic action causes the electrostatic repulsion between charged electrons in a QCA cell to synchronize the neighboring cells.
Two different polarizations (90° and 45°) will be produced as a result of this movement, leading to two different sorts of wires. Figure 3 illustrates the many sorts of wires.

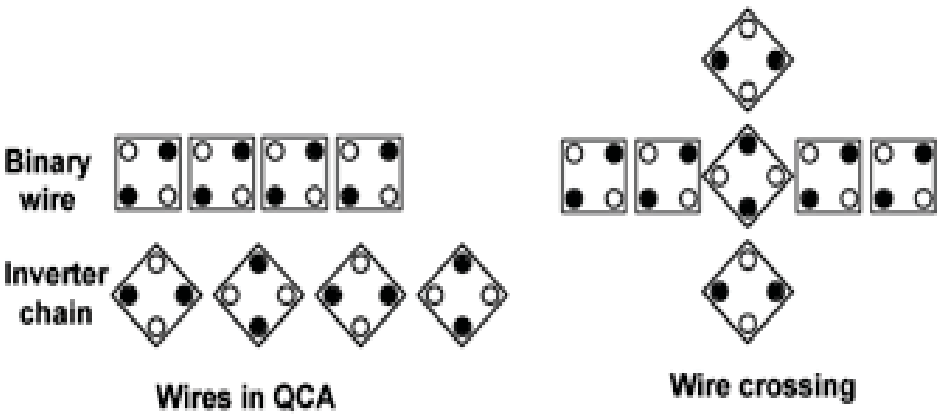


Fig.3. Types of QCA wires and wire crossing

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified ⁜ Impact Factor 7.105 ⁜ Vol. 9, Issue 8, August 2022

DOI: 10.17148/IARJSET.2022.9823

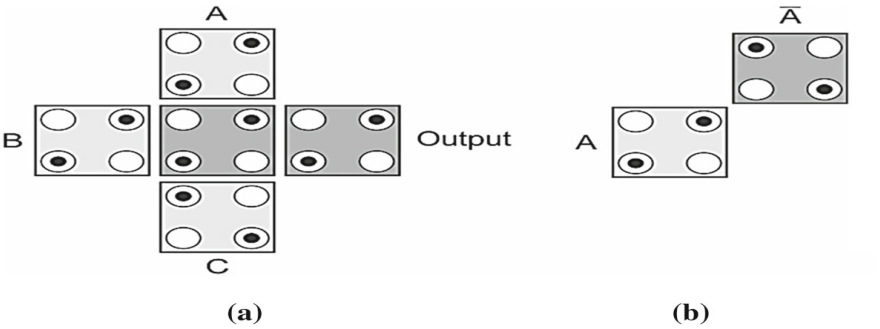


Fig 4. a) QCA wires a. 90-degree chains QCA cells b) cells with a 45-degree inverted chain

fig. 4. a shows a basic wire binary created by cells employing similar polarisation to convey logical "0" or "1". When designing the layout of an inverter chain, angles are avoided while drawing metal lines, as seen in Fig. 4b. Both building electronic circuitry, and connecting two separate blocks combined can be done using the same QCA cell.

B. QCA CLOCKING

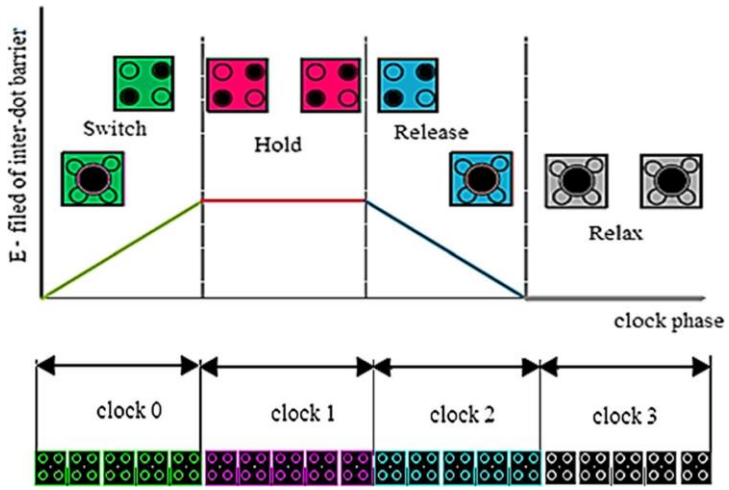


Fig. 5. 4 types of clocking phase of QCA

Any digital circuit's heart is its clock. The clock has a significant impact on how well a circuit performs.
The QCA technology clock serves the dual purposes of providing power and synchronization. To determine the direction of the cells, the circuits must be synchronized. The 4 types of clock zones, are as follow clock 0, clock 1, clock 2, and clock 3, are contained in a single QCA clock cycle.

Even though there is just a 180 degree phase difference between the nearby clock zones , it is 90° between the two succeeding clock phases. relax, hold, release, and Switch are the four clock phases or zones, and each phase has phase delay of 90° , as seen in Fig. 5. The cell is initially un-polarized while in the Switch phase, and Low barriers for inter-dot potential are used.
In keeping the condition of the neighboring (input) cell, the inter-dot potential obstacles include then gradually raised. This is the situation in which a computation is really carried out. Potential barriers are kept so high during the hold phase. Potential barriers are lowered and cells are relaxed to enter an un-polarized state during the release phase. Finally, the Potential obstacles are few, the cells are unpolarized, and they are in a relaxed state. Potential barriers between adjacent quantum dots can be managed via QCA clocking.

C. QCA GATES

Majority voter (MV) and NOT gates are the primary logical gates in QCA, as compared to the fundamental logical gates in conventional logic circuits, which are AND, OR. As depicted in fig. 3, a five cells can be used to make an MV gate. Because majority of all input polarities are factors that affect the polarity of the MV output, The MV's logic equation is

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified ⁜ Impact Factor 7.105 ⁜ Vol. 9, Issue 8, August 2022

DOI: 10.17148/IARJSET.2022.9823

MV of (X, Y, Z) = XY+YZ+ZX. (a)

An AND gate will be the result of setting one of MV's inputs to "0." One of the MV inputs set to "1" results in an OR gate as shown in below equations.

MV (0, Y, Z) = YZ. (b)

MV (1, Y, Z) = Y + YZ + Z = Y+Z. (c)

NOT gate design presented in below Figure. Furthermore, it is obvious that more cells are required for the implementation of a NOT gate than an MV.

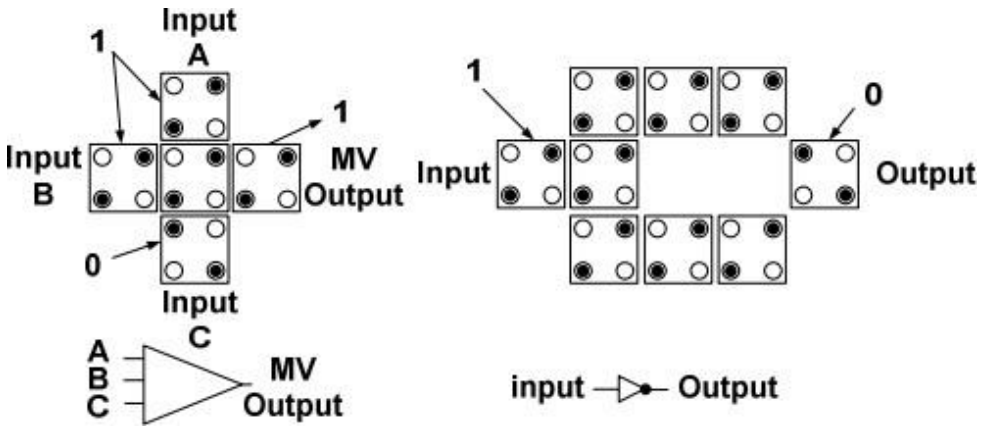


Fig.6. MV gate and not gate

III. IMPLEMENTAION OF FLIP-FLOPS

Sequential circuits called flip-flops have an output that depends on both the input's most recent value and the output's most recent value. This one-bit binary storage device may store binary data in the form of either a "1" or a "0." In this study, the SR flip- flop and three most popular types of flip-flops: T, D, and JK flip-flops were designed in this paper by making use of QCA tool.

A. SR Flip-Flop

The S-R flip-flop circuit has two outputs, Q and Qbar and two inputs, SET and RESET as shown in below figure. The other two inputs, S and R, use the clock pulse input as an enable input.

Figure 10. a shows the SR flip-flop diagram, and the implemented SR flip-flop layout using QCA technology is shown in fig 7. b.

The operation of the SR flip-flop is shown in the waveforms.

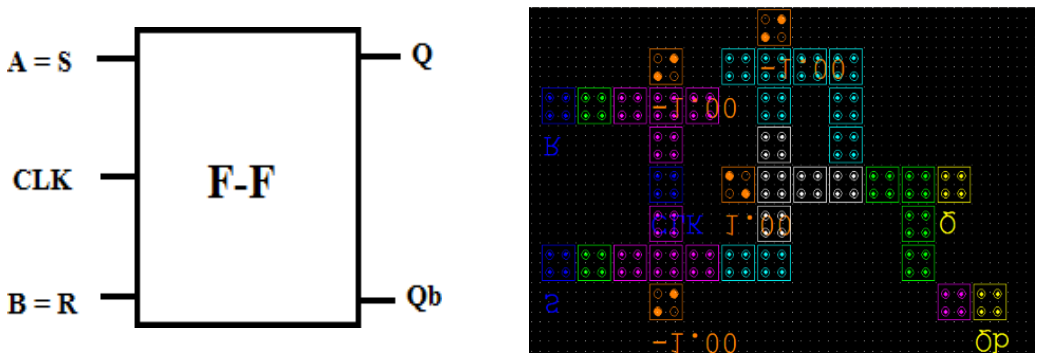


Fig.7. (a) SR flip-flop block diagram, (b)layout diagram of SR flip-flop

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified ⁜ Impact Factor 7.105 ⁜ Vol. 9, Issue 8, August 2022

DOI: 10.17148/IARJSET.2022.9823

B. D Flip-Flop

Due to the delay it introduces between input and output, the D flip-flop is named as the Delay flip-flop.
Figure 8. a shows the D flip-flop diagram, and the implemented D flip-flop layout using QCA technology is shown in fig8. b.
The operation of the D flip-flop is shown in output.

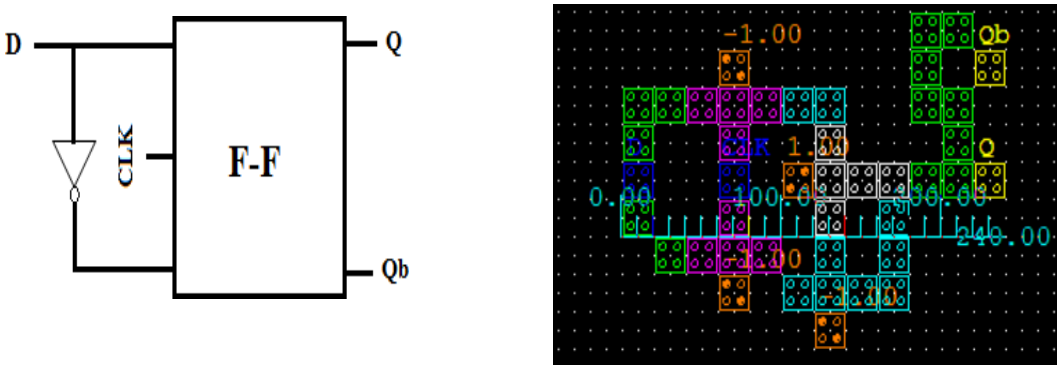


Fig.8. (a) D flip-flop block diagram, (b) layout diagram of D flip-flop

C. JK Flip Flop

JK flip-flop overcomes the SR flip-flips drawback. The J and K's inputs serve as inputs S and R, respectively, to setting and resetting the flip- flop. Results of the flip-flop is toggle, or move to its opposite state, when J=K=1.

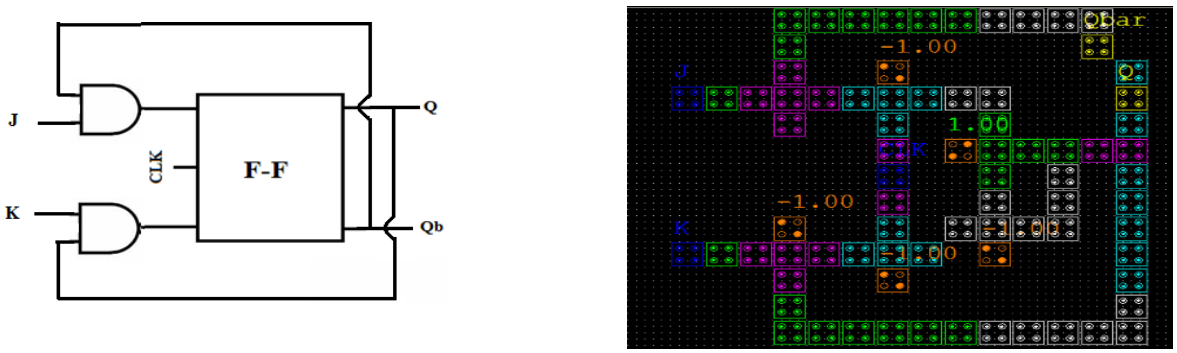


Fig.9. (a) JK flip-flop block diagram from, (b) Layout design of JK flip-flop

Figure 9.a shows the JK flip-flop diagram, and the implemented JK flip-flop layout using QCA technology is shown in fig9. b.
The operation of the JK flip-flop is shown in the output waveform.

D. T Flip Flop

The T toggle flip-flop, which only has two outputs, is another straightforward flip-flop (Q and Qb), a clock input, and a single data input (T). By coupling the J-K flip-J-K flop's inputs, the T flip-flop is designed. The ability to "toggle" or complement its state gives rise to the moniker "T," which is also used to refer to one input flip-flop. Here, we connected together the inputs both J and K by assuming that they are both T.

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified ⁜ Impact Factor 7.105 ⁜ Vol. 9, Issue 8, August 2022

DOI: 10.17148/IARJSET.2022.9823

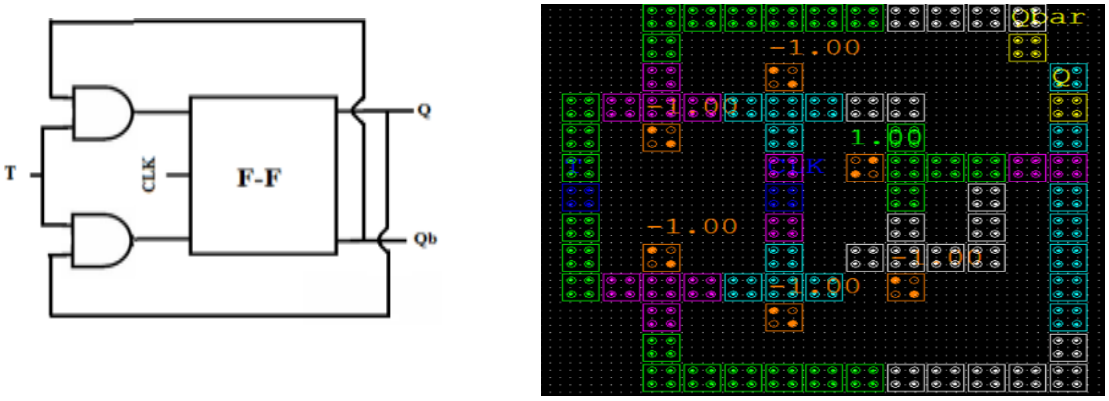


Fig.10. (a) T flip-flop block diagram, (b)Layout design of T Flip-Flop

Figure 10.a shows the T flip-flop diagram, and the implemented T flip-flop layout using QCA technology is shown in the fig10. b.
The operation of the T flip-flop is shown in the output waveform.

IV. IMPLEMENTAION OF DET- FLIP-FLOPS

Flip-flop-based circuits often run on the clock's active edge. The data may not change at every edge of the clock, which could lead to a higher power consumption as a result of this technique. Dual edge triggered (DET) based QCA circuits are created to prevent unnecessary transition. We used QCA technology to construct DET flip-flops such the SR, J K, D, and T flip-flops.

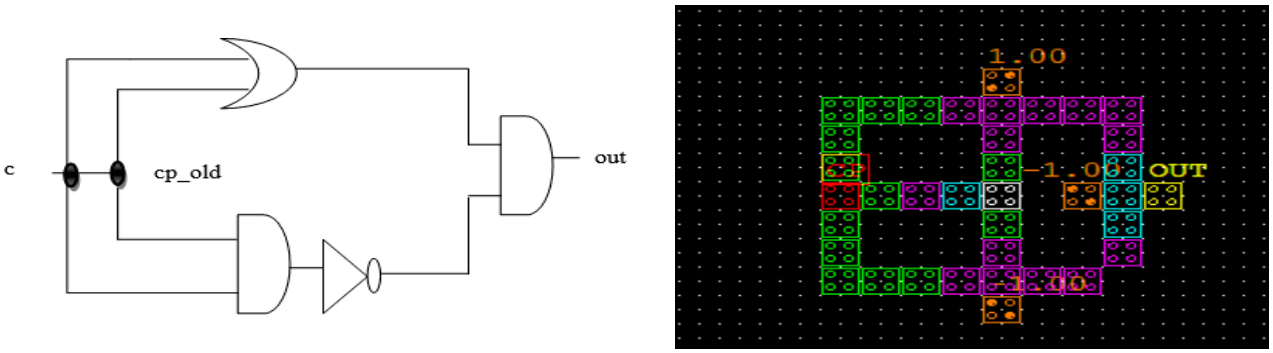


Fig.11. (a). Circuit diagram of dual edge trigger (b). QCA layout design of a dual edge trigger

In the figure 11.a shows the dual edge trigger diagram, and QCA layout design of a dual edge trigger is shown in the fig11.b.

A. DET BASED SR FLIP-FLOP

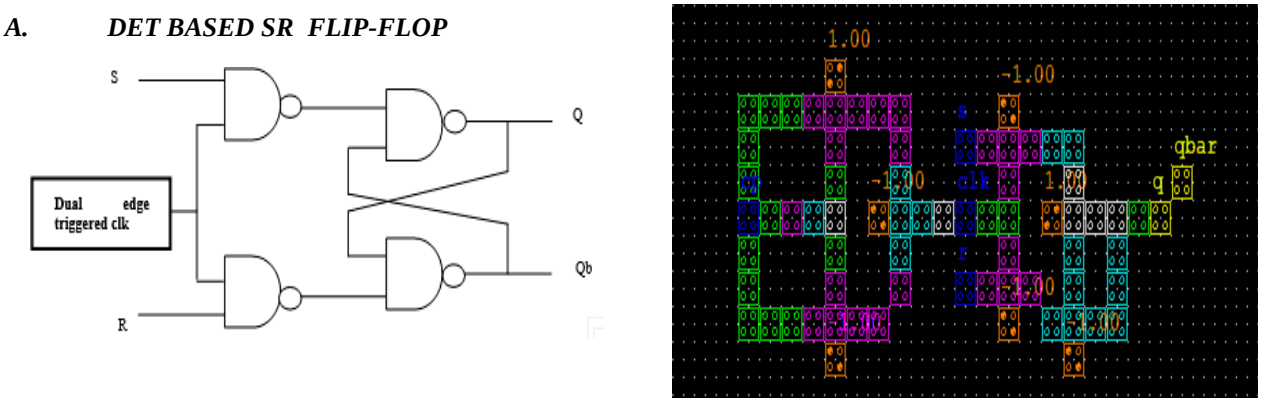


Fig.12. (a) Circuit diagram of dual edge trigger SR flip-flop (b). QCA layout design of a dual edge trigger SR flip-flop

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

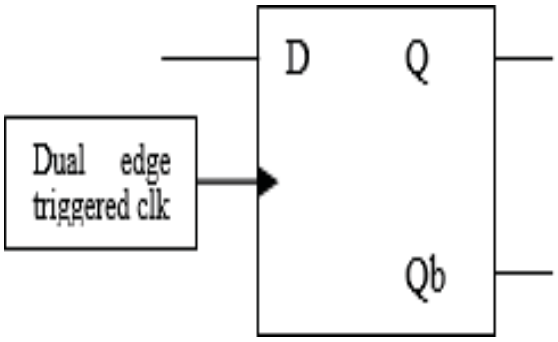
International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified ⁜ Impact Factor 7.105 ⁜ Vol. 9, Issue 8, August 2022

DOI: 10.17148/IARJSET.2022.9823

Figure 12.a shows the dual edge trigger SR flip-flop diagram, and the QCA layout design of a dual edge trigger SR flip flop is shown in Figure 12.b. The operation of DET based flip flops is the triggering at both the edges of the input clock, and we have the output of the flip flop on both the edges.

B. DET BASED D FLIP-FLOP



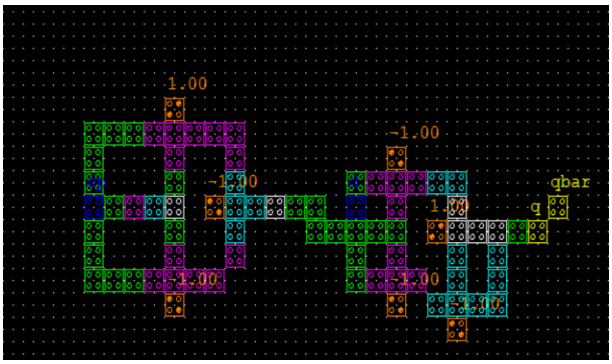
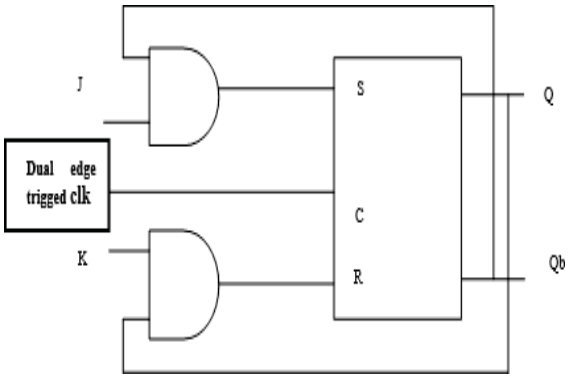


Fig.13.(a) Circuit diagram of dual edge trigger D flip-flop (b) QCA layout design of a dual edge trigger D flip-flop

Figure 13.a shows the dual-edge trigger D flip-flop diagram, and the QCA layout design of a dual-edge trigger D flip-flop is shown in fig.13.b. The operation of DET-based flip flips is the triggering at both the edges of the input clock and we get the output of flip flops on both the edges.

C. DET BASED JK FLIP-FLOP



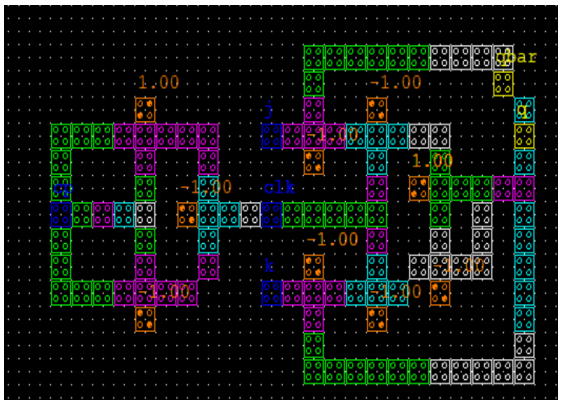


Fig.14. (a) Circuit diagram of dual edge trigger JK flip-flop (b) QCA layout design of a dual edge trigger JK flip-flop

Figure 14. a shows the dual edge trigger JK flip-flop diagram, and the QCA layout design of a dual-edge trigger JK flip flop is shown in the fig14. b.

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified ⁜ Impact Factor 7.105 ⁜ Vol. 9, Issue 8, August 2022

DOI: 10.17148/IARJSET.2022.9823

D. DET BASED T FLIP-FLOP

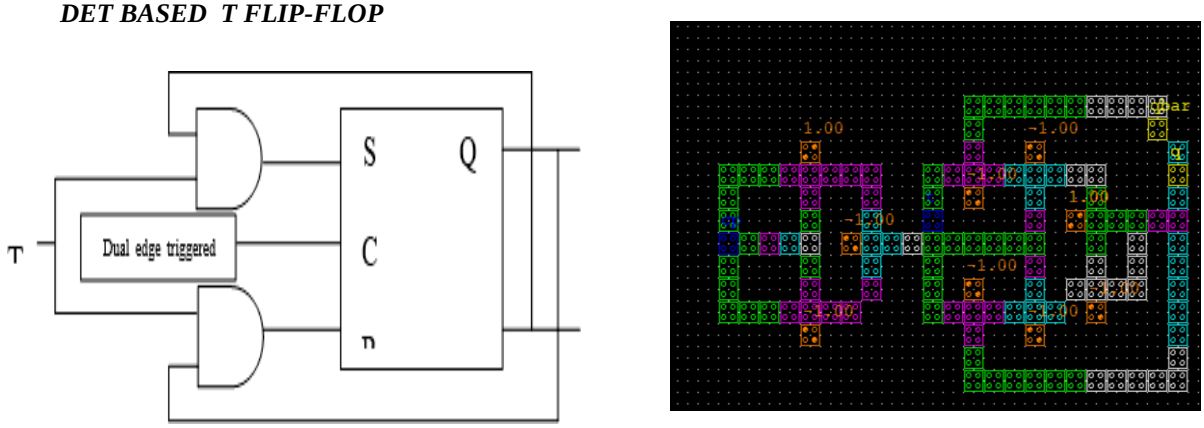


Fig.15. (a) Circuit diagram of dual edge trigger T flip-flop (b) QCA layout design of a dual edge trigger T flip-flop

Figure 15. a shows the dual edge trigger T flip-flop diagram, and the QCA layout design of a dual-edge trigger T flip flop is shown in the fig15. b.

V. RESULTS AND DISCUSSION

Simulation results of QCA flip-flops are shown below.

A. SIMULATION RESULTS OF QCA BASED SET FLIP-FLOPS

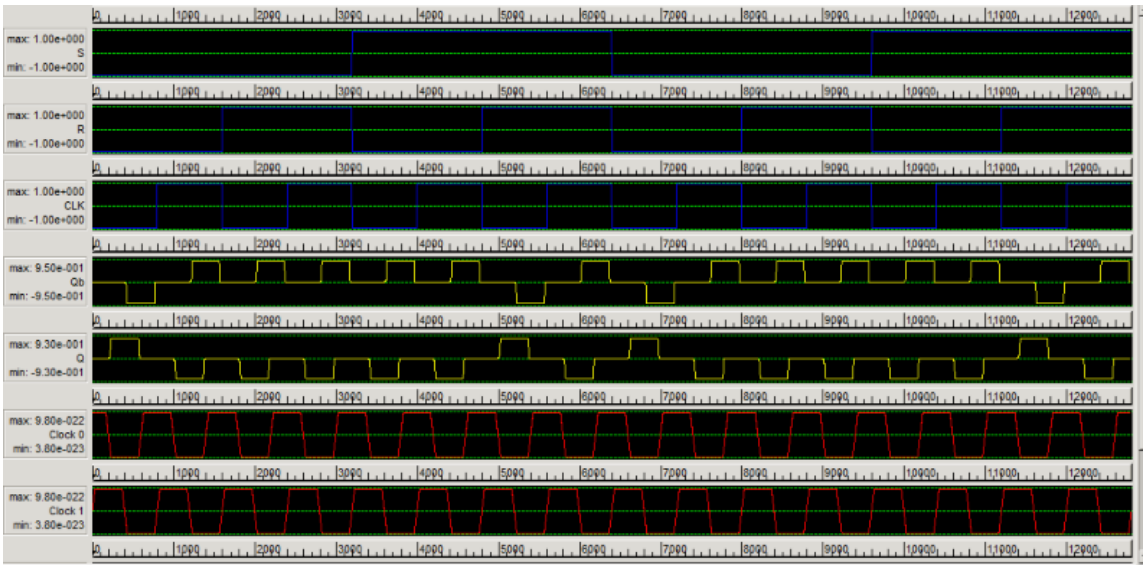


Fig.16. (a) SR flip-flop simulation result

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified ⁜ Impact Factor 7.105 ⁜ Vol. 9, Issue 8, August 2022

DOI: 10.17148/IARJSET.2022.9823

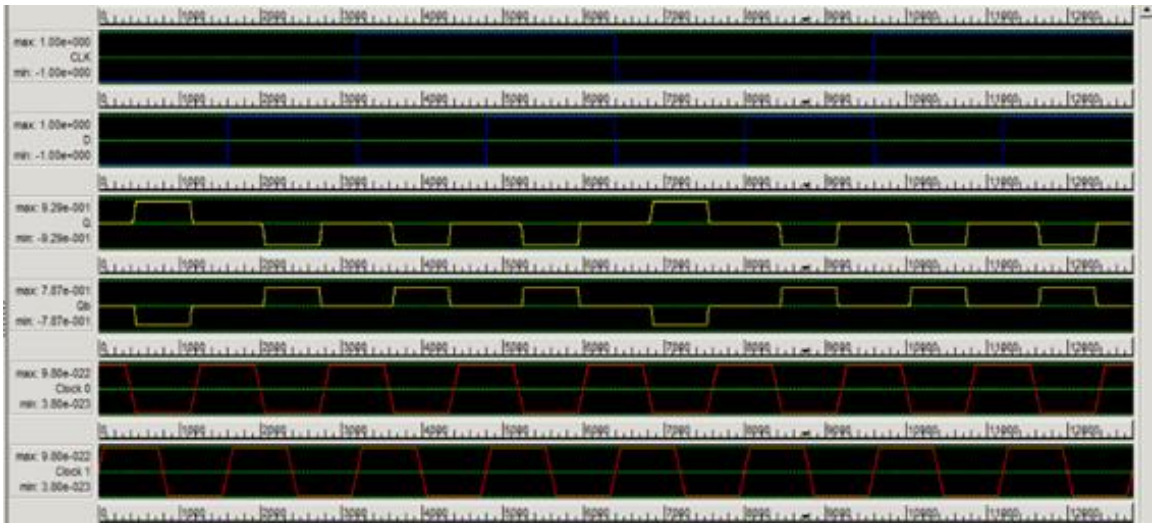


Fig.16. (b) D flip-flop simulation result

The simulation result of SET flip flops is shown in figures 16.a. and 16.b. of both the SR and D flip flops. We got the output of both the flip-flops successfully.

B. SIMULATION RESULTS OF DET BASED FLIP-FLOPS

The simulation results of DET-based flip flops are shown in Figures 17.a. and 17.b. for both the SR and D flip flops. We got the output of both the flip flops successfully, and we come to know that the area consumption is less and the switching speed is high.

The DET-based flip flops got the output on both edges, i.e., on positive and negative edges, as shown in the waveform below.

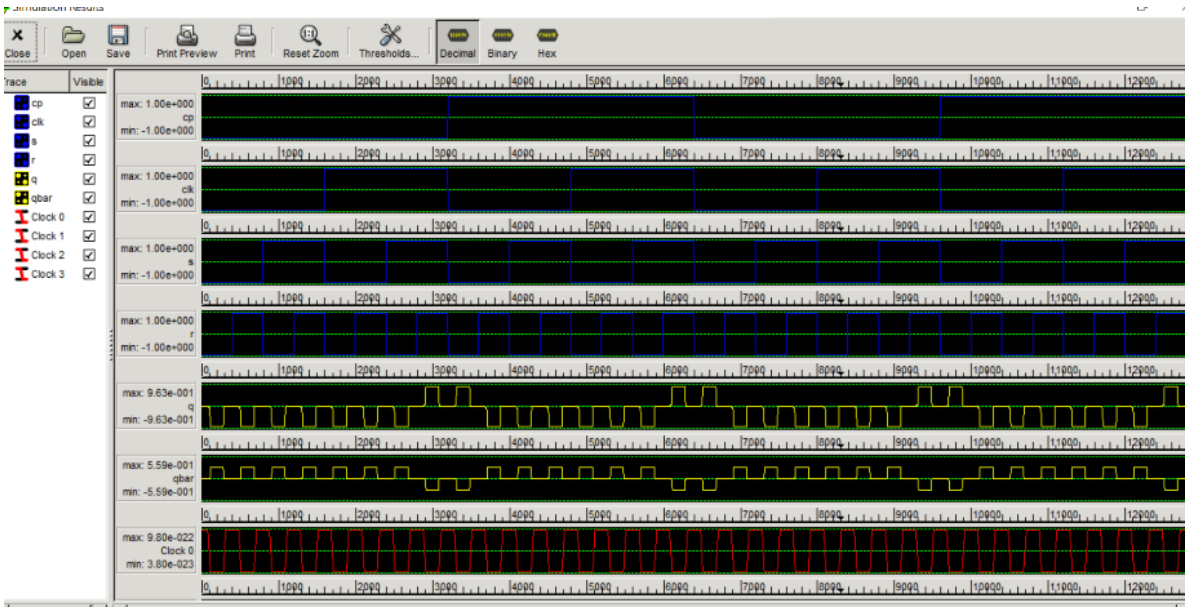


Fig.17. (a) DET SR flip-flop simulation result

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified ⁜ Impact Factor 7.105 ⁜ Vol. 9, Issue 8, August 2022

DOI: 10.17148/IARJSET.2022.9823

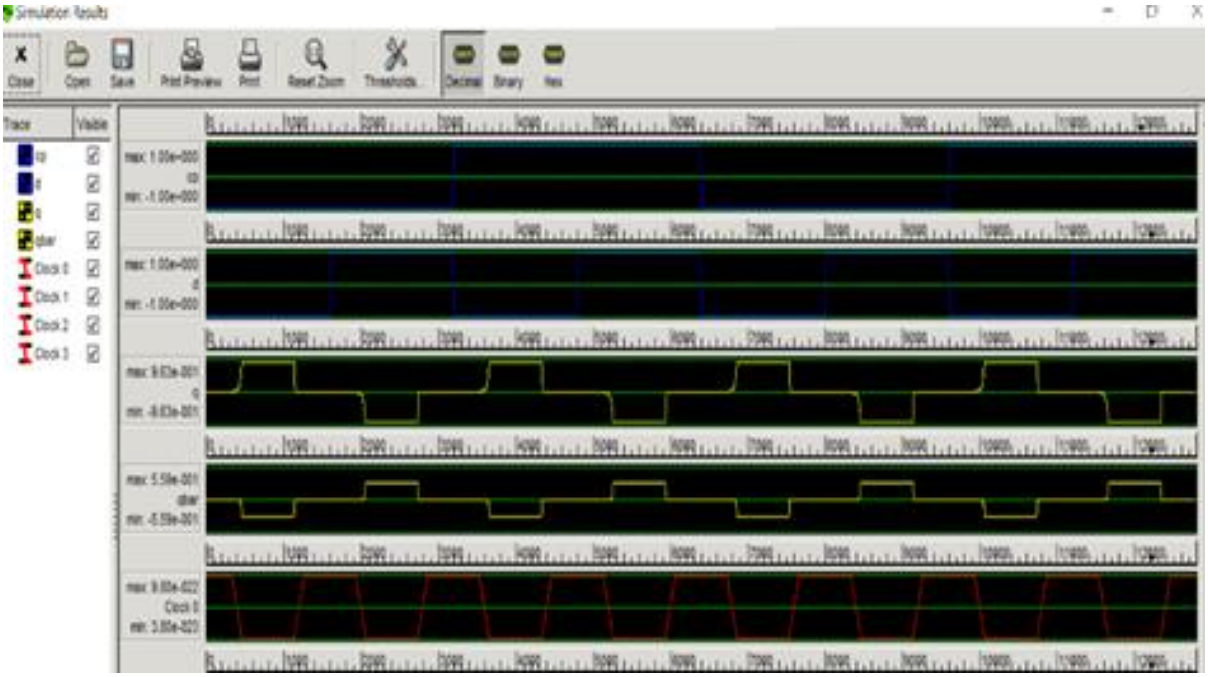


Fig.17.(b) DET D flip-flop simulation result

QCA based Basic gates and flip flop are constructed and analyzed using QCA Designer tool. We successfully get the output result of all the DET flip-flops, and we have seen that the DET JK flip-flop, D flip-flop, S-R flip-flop and T-flip-flop are analyzed and it is better than the CMOS technology and single edge trigger circuits as shown in paper.

TABLE 1

COMPARISON BETWEEN FLIP FLOPS WITH A SINGLE EDGE TRIGGER AND FLIP FLOPS WITH A DUAL EDGE TRIGGER

Type	Cell	IP/OP	MV	INV	CO	Length	Width	Area NM^2	Total energy Dissipation(eV)
Single Edge Based Flip-flops									
SR	38	5	4	2	2	258	158	40,764	9.30e-001
D	43	4	4	3	2	240	180	43,200	7.87e-001
JK	78	5	6	2	2	278	258	71,724	9.51e-001
T	81	4	6	2	2	257	258	66,306	9.51e-001
Dual Edge Triggered Based Flip-flops									
SR	71	5	7	3	2	419	178	74,582	5.59e-001
D	78	4	7	3	2	479	200	95,800	5.59e-001
JK	122	6	9	3	2	460	260	119,600	9.51e-001
T	124	4	9	3	2	460	259	119,140	9.51e-001

QCA-based flip flops are constructed and analyzed using the QCA Designer tool. From table 1, the results show that DET Based D FF consume less power and area when compared to other flip-flops.

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified ⁜ Impact Factor 7.105 ⁜ Vol. 9, Issue 8, August 2022

DOI: 10.17148/IARJSET.2022.9823

VI. CONCLUSION

To resolve the problem of CMOS ICs with respect to physical limits, QCA circuits provide a better solution in terms of performance, like area, power, and switching speed. We have designed basic gates, SR flip-flop, D flip-flop, JK flip-flop, and T flip-flop using QCA technology. Then we will design the DET-based flip-flops. The design with DET is found to produce better results with respect to power consumption when compared with other designs. Hence, it is better to use DET-based flip-flops, and in the future, we can design complex digital circuits.
Hence we have compared the DET flip-flops and single-edge flip-flops in paper [9] and we have concluded that the DET flip-flop has less power consumption.

REFERENCES

[1] J. Huang, M. Momenzadeh, F. Lombardi, “Design of sequential circuits by quantum-dot cellular automata”, Microelectr. J., vol.38, pp.525–537, 2007.

[2]Abbas Shahini Shamsabadi, Behrouz ShahgholiGhahfarokhi, Kamran Zamanifar, Naser Movahedinia , ”Applying inherent capabilities of quantum-dot cellular automata to design: D flip-
flop case study.” Journal of Systems Architecture, vol 55, no.3, 2009.

[3]Jagarlamudi, Hema Sandhya, Mousumi Saha, and Pavan Kumar Jagarlamudi. "Quantum dot
cellular automata based effective design of combinational and sequential logical structures." World Academy of Science, Engineering and Technology, vol.60, pp.671-675, 2011.

[4]Torabi , Mohammad. "A new architecture for T flip flop using quantum- dot cellular automata." In 2011 3rd Asia Symposium on Quality flops.

[5]Xiao, Lin-rong, Xie-xiong Chen, and Shi-yan Ying. "Design of dual- edge triggered flip-flops based on quantum-dot cellular automata." Journal of Zhejiang University SCIENCE C 13, vol.5,
pp.385-392, 2012.

[6]Int. J.Adv.Sig.Img.Sci, Vol. 3, No.2, 2017 QCA DESIGN FOR 4-BIT ASYNCHRONOUS DOWN COUNTER Dr. Thivya K.S, Department of Electronics and Communication Engineering, Easwari Engineering College, Chennai, India.

[7]Zhang, Yongqiang, Guangjun Xie, and Hongjun Lv. "Dual-edge triggered JK flip-flop with
comprehensive analysis in quantum-dot cellular automata." The Journal of Engineering, vol. 7, pp. 354-359, 2018.

[8]Laajimi, Radhouane. "Nanoarchitecture of Quantum-Dot Cellular Automata (QCA) Using
Small Area for Digital Circuits." Advanced Electronic Circuits: Principles, Architectures and Applications on Emerging Technologies,vol. 67,2018.

[9]Ratna chakrabarty,Deepakkumarmahato”A Novel Design Of Flip Flop Circuits Using Quantum Dot Cellular Automata” Conference IEEE 2018.

[10]Quantum-Dot Cellular Automata Technology for High-Speed High-Data-Rate Networks Adepu Hariprasad1 · Sreenivasa Rao Ijjada2 Revised: 12 February 2019 / Accepted: 14 February 2019/ Published online: 29 April 2019.

[11]Design of 4-Bit Dual Edge Triggered Counter using Quantum DOT Cellular Automata BY M.Rajmohan, K.Sakthidasan @ Sankaran and T.Rasagna. 2020.

