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Novelty method for control PMOS unidirectional current flow

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Abstract: If we want to make the current of circuit to flow in only unidirectional. Typically, a diode would be adopted to control the current flow in only one direction that is from the high voltage side flows to the low voltage side. Traditionally, the voltage drop of a diode is about 0.6V. However, when a forward voltage is applied to the diode, the voltage drop across the diode actually exceeds 1V. If the forward current through the diode is about 10A, that will result the power loss from the diode is about 10W. In order to reduce this power consumption, another approach can use the MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) to replace the diode to reduce conduction loss. But, when the MOSFET is turned on, it's current can flow in both directions. This paper proposed a novelty method for control PMOS unidirectional current flow. Only a few passive components are required, the PMOS will be driven to conduct only one direction, which provides a simple and economical solution for circuit application.

Keywords: MOSFET, diode, unidirectional, forward current, forward voltage.

I. INTRODUCTION

In circuit applications, sometime it is necessary to implement that the current be only conducted in one direction [1-4]. Traditionally, it is the most common implement to connect a diode in series on the circuit. However, a typical diode drop is 0.6V. For reduce the voltage drop of a diode, the Schottky diode be used frequently.

Disadvantages of adopt a Schottky diode for unidirectional current flow include [5]:

- Forward voltage drop: The typical voltage drop for Schottky diode is about 0.2V~0.4V, although lower than the general diode. But still cause power loss when high load current.
- Thermal management: Power losses are usually mostly converted to heat loss then requires additional heat sink or heat dissipation which increasing space and total cost.
- Power consumption: When exist the high load current and forward voltage drop which result conduction loss with low efficiency.
- Reverse leakage current: When the Schottky diode is reverse biased, although it is turned off, the drift motion of minority carriers will result a reverse current flowing from the negative terminal of the diode to the positive terminal of the diode. This reverse current is generally known as leakage current. This leakage current will cause unnecessary power loss in the circuit and reduce the overall power efficiency of the circuit.

In order to reduce the conduction loss of the diode, another typical approach is to adopt synchronous rectification [6-8] at the output. The MOSFET (N type named NMOS or P type named PMOS) is adopted to replace the rectifier diode at the output. This will effectively reduce the conduction loss of the output. But the basic characteristics of MOSFET are the NMOS is normally opened and need driving positive voltage in gate (G) and source (S) pin to turn it on. Comparatively the PMOS need driving negative voltage in gate and source pin to turn it off. However, the main problem is that MOSFET is bidirectional current can flow. But in some circuit applications we need the current to flow only in one direction. It is impossible to achieve the goal of undirectional current flow by just using MOSFET without other special designs. The most common method is to use an additional control IC to control the MOSFET to be undirectional. Merely that requires a higher total cost. This paper proposes a novel method to control PMOS for undirectional current flow.



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II. OPERATING PRINCIPLES

The proposed method for PMOS only unidirectional current flow is shown in Fig. 1. It is included a DC voltage (V_{in}), one PMOS (M_1), three PNP BJT (Q_1 , Q_2 , Q_3), one NPN BJT (Q_4), one diode (D_1), one load resistor (R_9), and some bias resistor ($R_1 \sim R_8$). The key to design of this method is to make the voltage at point A greater than the voltage at point B by about 0.6~0.7V. Since M_1 is a PMOS, suppose it be turned off by V_{out} and R_8 at the beginning. When $V_{in}>V_{out}$, the Q_1 be turned on, and the Q_2 also be turned on. When the voltage at point A greater than the voltage at point B by about 0.6~0.7V, the diode (D_1) will be turned on. Then the Q_3 be turned on, consequently the Q_4 also be turned on. Then the gate pin of M_1 will be pull-low to ground, that make sure M_1 is turned on.

On the contrary, When $V_{in} < V_{out}$, the Q_1 will be turned off, and the Q_2 also be turned off. Owing to the voltage at point A don't greater than the voltage at point B about 0.6~0.7V, the diode (D₁) also be turned off. Then the Q₃ be turned off, the Q₄ also be turned off. Then the gate pin of M₁ will be pull-high to V_{out} by R₈, that make sure M₁ is turned off.

At the result, the PMOS (M_1) will only be only one direction conducted, that is, it will only allow current to flow from drain (D) to source (S) of M_1 , but not from S to D.

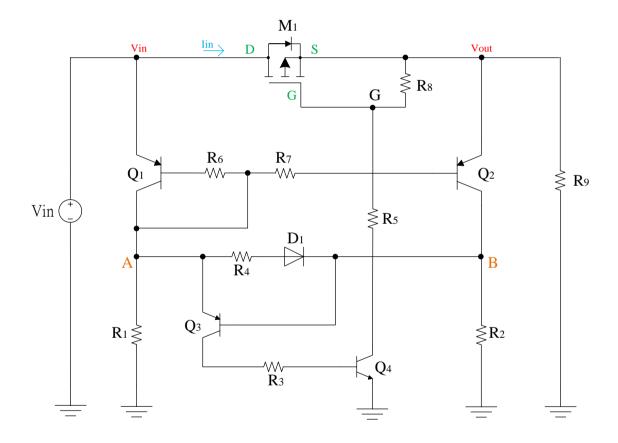


Fig. 1 The proposed method for PMOS only unidirectional current flow.

Basically, the above circuit adopt to detect whether there is current flowing from node A to node B. And it's according to generate a voltage signal to turn on or off the transistor Q_4 . When the transistor Q_4 is turned on, there is a current path between the input terminal and the output terminal of M_1 . However, when the transistor Q_4 is turned off, there is an open circuit between the input terminal and the output terminal of M_1 . In this way, the entire circuit can control the on or off of M_1 .

The feature provided by this method is adopt PMOS transistor instead of a diode. Compared with the diode, the voltage drop from the PMOS transistor is much smaller than the voltage drop from the diode, so the power loss generate is smaller a lot. Furthermore, since the diode only has two pins, when it is applied to unidirectional conduction, it is only controlled to turn on and off according to the voltage of its two pins. However, the PMOS transistor has three pins. When it is used for unidirectional conduction, the circuit can generate a voltage signal to the PMOS as a control logic to control the on and off of the PMOS transistor. Such control is more flexible and precise.



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III.DESIGN EXAMPLE

A design example is shown in in Fig. 2. Here the V_{in} is 19V. The resistance value (R_{ds_ON}) between the drain and source of M_1 during operation (ON) is 3.26m Ω . If I_{in} is about 3.064A, then V_{out} is 18.99V. Owing to V_{in} is 19V, then the base pin of Q_1 is 18.3V (refer to \oplus of Fig. 2). The V_{out} is 18.99V, then the base pin of Q_2 is 18.29V (refer to \oplus of Fig. 2). When the I_{B_Q1} is designed in 4.85 μ A and R_6 is 160k Ω , then the voltage at point A is 17.52V (refer to \oplus of Fig. 2). On the other hand, due to the voltage at point A is 17.52V, then the base pin of Q_3 is 16.89V (refer to \oplus of Fig. 2). When the voltage drop at D_1 is 0.6V, the current of I_{R4} is (17.52-0.6-16.89)V/1k Ω =30 μ A. Owing to the I_{B_Q1} is designed in 4.85 μ A, then I_{E_Q1} is 909.5 μ A, I_{C_Q1} is 904.6 μ A. The I_{R7} is (18.29-17.52)V/200k Ω =3.85 μ A, then the sum of currents at \oplus is 8.709 μ A. The current feed into point A is 913.35 μ A, and I_{R1} is 796.36 μ A. The emitter current of Q_3 is 86.98 μ A, the collector current of Q_3 is 86.51 μ A. And the Q_4 is turned on, the gate pin of M_1 is pulled low then the M_1 is turned on.

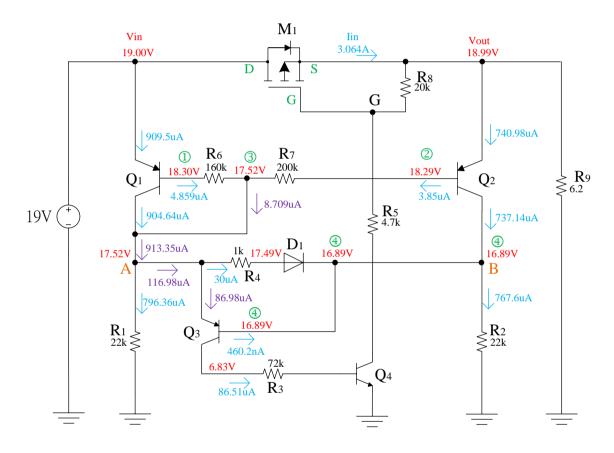


Fig. 2 A design example.

It can be seen from Fig. 2. If at any time the V_{in} is less than V_{out} then the voltage at point A unable greater than the voltage at point B by about 0.6~0.7V. At this time, the diode D₁ cannot be turned on, that is, no current will flow through D₁. In other words, no current will flow through Q₃. Then Q3 will be turned off, its accompany that Q₄ will also be turned off. When the Q₄ be turned off, the gate pin of M₁ will be equipotential to V_{out} then the M₁ will be turned off. The above process will ensure that M₁ only conduct unidirectional current flow. It would not be bidirectional conduction current like traditional PMOS.

The method presented in this article can be implemented with only a few transistors and resistors. No need for control IC or other controllers at all. This will effectively reduce the overall implementation cost. In addition, it should be noted that considering the voltage-current characteristics of the diode D_1 . In this design example, the correction resistor R_4 can be placed between the transistors Q_3 and D_1 to adjust the sensitivity of the transistor Q_3 depends on user application needs.



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IV.SIMULATION RESULTS

In order to verify the feasibility of the proposed method in this paper. Design example based on the above chapter is model for simulation. From the Fig. 3 show that when V_{in} > V_{out} , the I_{in} is conducted and the current flows forward. On the contrary, when V_{in} < V_{out} , the I_{in} is not conducted and the current equal to zero.

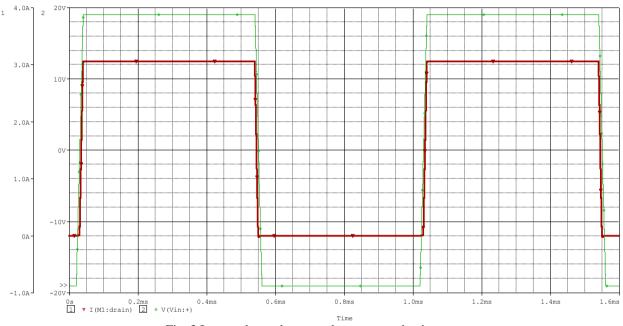


Fig. 3 Input voltage change and current conduction or not.

On the other hand, the peripheral current waveforms are shown in the Fig. 4. It can be clearly seen that when $V_{in}>V_{out}$, the peripheral currents are turned on and appeared. On the contrary, when $V_{in}<V_{out}$, the peripheral currents are turned off and disappeared. This again verifies the effectiveness of the proposed method in this paper.

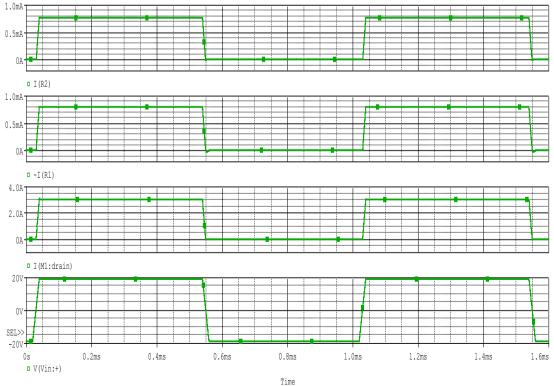


Fig. 4 Peripheral current waveforms.

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Of course, there will be some noise and non-ideal characteristics in practical applications. However, this does not affect the control logic proposed in this paper that it still control PMOS unidirectional conduction.

V. CONCLUSION

A novelty method for control PMOS unidirectional current flow is proposed in this paper. Only need passive components to design then make the PMOS only unidirectional conduction. Such a solution effectively makes the current only unidirectional flow and don't need to use traditional diode implementation method with consequently high conduction loss. The principle of operation and a design example are shown. The simulation results further prove the feasibility of the proposed method in this paper.

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