IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified ⁜ Impact Factor 7.12 ⁜ Vol. 9, Issue 10, October 2022

DOI: 10.17148/IARJSET.2022.91012

SAR A/D Converter to FPGA Interfacing for Analog Sensor Data Acquisition

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Abstract: In this paper a methodology to interface FPGA with SAR A/D converters has been stated. A simulation result for two different ADCs using the proposed interfacing methodology has been presented. This paper also comes up with a UART transmitter module designed for hardware implementation in which an 8-bit resolution A/D converter has been interfaced with FPGA using the methodology given in this paper. In hardware implementation A/D converter acquires analog data from LM35 temperature sensor and the conversion result is sent via the proposed UART module and visualized on PC using Tera-term software.

Keywords: Sensors, ADC, Baud Rate, FPGA, Interfacing.

I. INTRODUCTION

Sensors have their applications throughout the engineering sector. On variation of the physical attributes they measure, sensors generate electrical signals. Based on the nature of the output signals they are broadly classified as analog or digital. Analog sensors provide specific values along some scale. They are widely used in applications where precise feedback is required rather than just the status of the signal. There are many uses for analogue sensors, ranging from basic thermometers to mission-critical applications like satellites where monitoring the data from these sensors is important for its operation and control.

Since the core processor of every electronic or embedded system processes data in digital form therefore the analogue output from these sensors needs to be converted into their digital equivalent for which analogue to digital converters are used. SAR A/D converters (Successive approximation register analogue to digital converters) are the most popular because they employ digital logic that converge the analogue input voltage to the closest value. They are typically implemented in data acquisition systems where data is generated by many sensors such as satellites, medical imaging, industrial process control, optical communication systems.

Accessing and analysing data is one of the most needed topics in every field of engineering. Data acquisition system is used for different purposes like simultaneous recording of data from hardware interfaces and generating digital/ analogue data for testing [1]. In this section application of data acquisition in distinct use cases has been reviewed. In [2], Saputra et al have proposed an Electroencephalography data acquisition system based on FPGA (Field Programmable Gate Array) Zed board. The system uses two chips of 24-bit Delta Sigma A/Ds connected to electrodes made up of noble metals. The standard communication. protocol between A/D converter and FPGA Zed board is SPI. The result is given to the computer through serial data protocol.

In [3], Yao-Hua proposes a data encryption/decryption system based on FPGA in the field of industry. The system has a field encryption board and one host decryption board. The field encryption board is responsible for data acquisition. The data acquisition system has ADC0809 interfaced with FPGA through a 7 state, state machine design. After the encryption of acquired data in an FPGA, it is sent to the host decryption board through the UART protocol.

In [4], Adhikary et al. have proposed a data acquisition and monitoring system. Yagi - Uda 7 element simple dipole antenna and folded dipole with reflectors are used. The signal is received from the detector and given to A/D for conversion and fed to FPGA. The signals are then compared and stored in the memory. Also, it guides the antenna in the direction of the signal received whether it is maximum or minimum.

From the above mentioned works it can be concluded that data acquisition has significance in diverse applications and considering this fact, a simple data acquisition system using interfacing of SAR A/D (Successive approximation register analogue to digital converters) converters with FPGA (Field Programmable Gate Array) has been given in this

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paper. The SAR A/Ds have been considered because of their low power consumption, high resolution, and accuracy. The methodology gives a two-state model for interfacing SAR A/Ds to FPGA. The data visualization can be done by sending it to computer using simplex UART (Universal Asynchronous Receiver Transmitter) transmission logic. This logic can be implemented in many applications for data acquisition, for example interfacing of AD7249 with FPGA can be utilized in cube satellite missions for acquiring data from sensors such as analogue sun sensor, NTC (Negative Temperature Coefficient) thermistors or analogue information sent from other subsystems. Along with the implementation of UART logic it can be utilized to check the performance parameters or doing pre-launch go/no go tests for these sensors. Our proposed method uses the FPGA resources in an optimized way.

II. DESIGN SCHEME

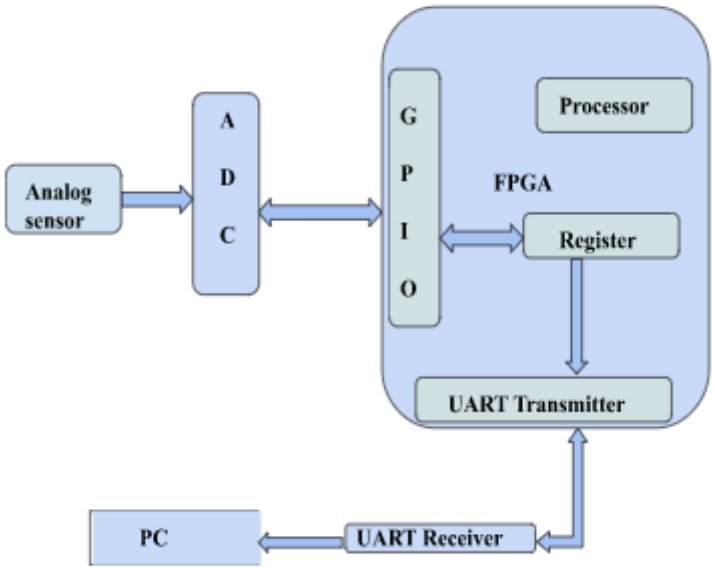

Fig. 1 Block Diagram of Design Scheme

As explained in section I, this paper discusses the methodology of interfacing SAR analogue to digital converters with FPGA for analogue sensors data acquisition and testing. The methodology of interfacing has been applied on a hardware system in which a low cost 8-bit resolution A/D converter, ADC0809 is used and analogue input from LM35 temperature sensor is given to it and the acquired converted data is sent through UART transmitter module designed on FPGA to PC where the result is visualized on Tera Term software as its ASCII equivalent. The block diagram of the design scheme for hardware implementation is shown in Fig. 1.

III. SOFTWARE MODULE DESIGNS

A. ADC Interfacing logic for FPGA

Interfacing is basically an exchange of signals. Usually, three types of control signals regulate the interaction between SAR A/D Converter and processor (FPGA in this case).

- START or CONVST: This is a trigger signal sent from FPGA to initiate the working of the subcircuits inside the A/D.
- Busy or End of Conversion: This signal is sent from ADC to indicate the status of the conversion process.
- Output Enable or RD: This signal is sent from FPGA to access the conversion result.

Even though the polarities and names of these signals may vary for different SAR ADCs (Analogue to Digital Converter), the fundamental concept is the same [5].

The interfacing module has been designed as a state machine that has two states, an initial state ‘init’ and conversion state ‘convert’. Before giving clock pulse to the module the signals that are to be sent from FPGA are set to the signal states as specified in the data sheet of ADC. Right at the first positive edge of the clock module is pushed into ‘init’ state.

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In the initial state the polarities of START or CONVST is changed for some specified duration of time and after that are brought back to the same signal states. This activates the ADC conversion circuit, and it in response sends BUSY or EOC signal. At the leading edge of BUSY or EOC signal the state of the module is changed to 'convert'. In this state the BUSY or EOC signal is monitored, and a condition is set such that once the polarity of signal gets changed, Output Enable or RD signal is sent for some duration and the conversion result is acquired parallelly through input ports of the FPGA and stored in the system register.

After this module again goes back to state 'init' to start a new conversion cycle. Fig. 2 gives flow chart for the logic. The pulse widths of the signals sent from FPGA should be according to the timing diagram specifications given in the data sheet of A/D converter being used. The duration of signals in 'init' and 'convert' states is controlled by running counters for certain number clock pulses.

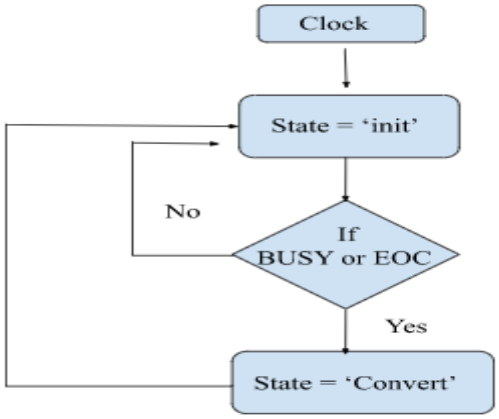

Fig. 2 Flow chart for ADC-FPGA interfacing logic

B. UART Transmitter module for Hardware Implementation.

UART [6] is a kind of universal serial data bus, used for asynchronous communication. The UART module has three components: Baud Rate generator, Transmitter Hold Register and Transmitter Module as shown in the block diagram in Fig. 3. Since UART is an asynchronous communication protocol thus no clock information is shared between the transmitter and the receiver which can lead to errors on reception. In order to solve this problem sampling technique is used where both the transmitter and the receiver sample a bit for N no of times. The most common sampling rate is 16 times baud rate, which means each bit is sampled 16 times [6].

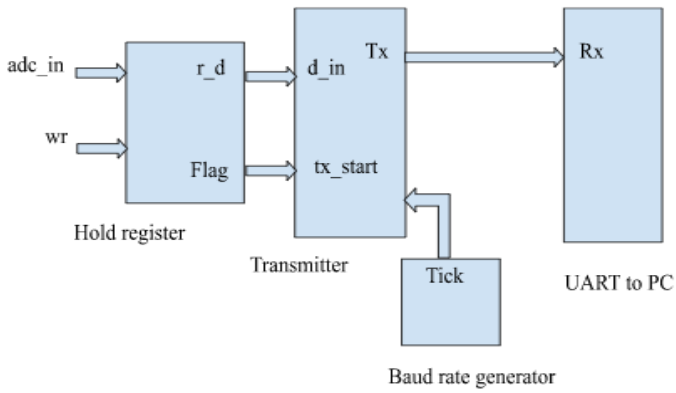

Fig. 3 UART Transmitter Block diagram

In order to generate a sampling clock, baud rate generator is used which is basically a frequency divider. The baud rate generator will have a mod-n [i.e. [System frequency] ÷ [Baud Rate×16]] counter [6]. Thus, after every n clock cycle a sample tick 'Tick' will be asserted.

The transmitter 'Hold register' is used for holding the conversion data. The transmitter module is designed as a state machine of four states: Idle, Start, Data, Stop, as in Fig. 4. When no clock signal is given the state is 'Idle' and it

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transmits logic signals 1. When the clock pulse is provided and a control signal 'wr' is given the data gets written from the FPGA register 'adc_in' to the 'Hold register' and a flag signal 'Flag' is raised in the hold register logic, this signal sets the 'tx_start' register in transmitter and triggers it to shift to 'Start' state. The transmitter remains in this state for 16 sample ticks and transmits a start bit of logic '0'.

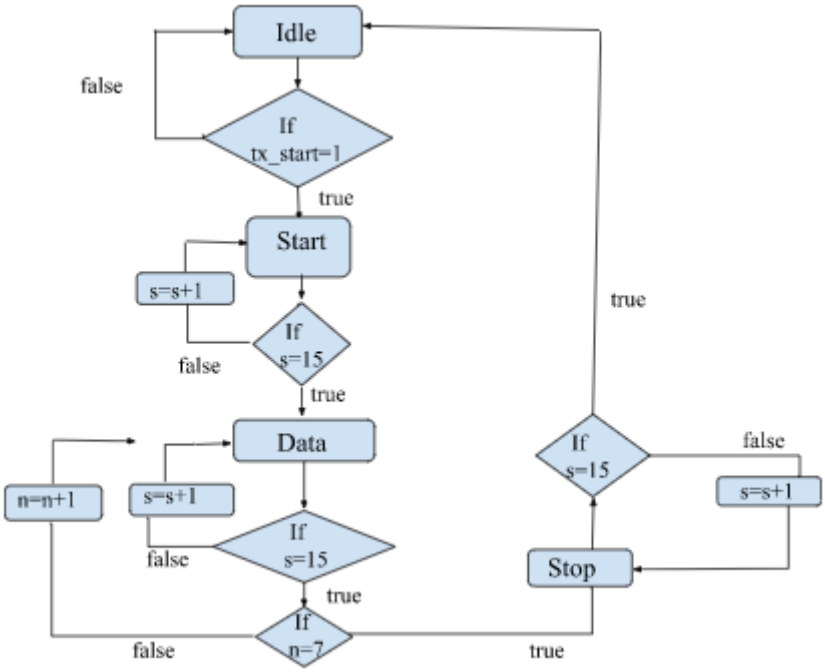

Fig. 4 Flow chart for Transmitter logic

After transmitting the start bit the transmitter moves to 'Data' state and one by one shifts out data bits from the hold register through logic output port 'r_d' to logic input port 'd_in' of transmitter. Each bit is shifted out through 'Tx' pin transmitter after every 16 sample ticks. A counter 's' is run in each state to count the sample ticks. In data state a counter 'n' gets incremented each time 's' reaches to 16 while shifting a data bit. When 'n' is equal to 8 the transmitter shifts to 'stop' state. In this state for 16 sample ticks, a stop bit '1' gets transmitted. The data is received through 'Rx' pin of receiving UART module connected to personal computer.

IV. HARDWARE IMPLEMENTATION

The hardware and software used in the implementation have been given in Testbed configuration and parameter initiation Table I. The schematic of the PCB in Fig. 6 shows the connections given to the AD0809 IC mounted on it. The supply voltage pin Vcc and reference voltage pin Vref of the IC are given voltage of 5 and 2.5 volts respectively from a dual power supply. The hardware setup for the implementation is given in Fig. 5.

The device has an 8-channel single ended analog signal multiplexer [7]. A particular input channel is selected by an on-chip address decoder [7]. The address is latched into the decoder on the low to high transition of the address latch enable (ALE) signal which is given from the zed-board. The analog data from LM35 sensor is given through input pin IN0 which is selected by connecting all the three address pins to ground thus a combination of '000' input is latched into the address decoder [7].

The LM35 gives an output signal of voltage [9]

$$Vout = 10mV/℃ \times T \quad (1)$$

Where T is temperature in ℃.

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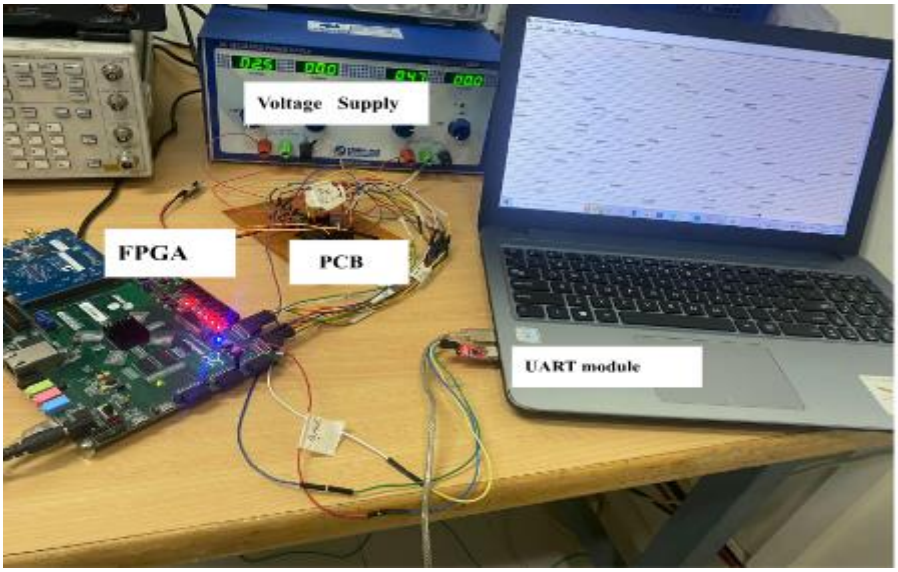

Fig. 5 Hardware set-up

TABLE I TESTBED CONFIGURATION AND PARAMETER INITIALIZATION

S.NO	Hardware	Software	Operating Frequency	Control signal initialization before clock pulse is given	Baud rate for UART
1.	Zed board (AVNET)	VIVADO for design implementation on Zed board in VHDL	100 MHz for Zed board	ALE: 0	38400 bps
2.	ADC0809	Tera term software for data visualization on PC.	500 kHz for ADC0809	Start: 0	
3.	UART MODULE			Output Enable: 0	
4.	LM35 Temperature Sensor				

Once the 'Start' signal is provided the ADC0809 starts conversion, 'EOC' gives status of signal conversion inside ADC and on receiving 'Output Enable' 8-bit conversion result is driven into Zed-board, parallelly through its 8 I/O pins.

The transmitter circuit on FPGA is initiated when the 'wr' signal that has been port mapped to one of the switches of the Zed board, is given to the transmitter hold register. The control signals are given out and received from the I/O pins of Zed board. Since AD0809 IC works on a 500 kHz external clock pulse. The clock signal is provided by applying frequency divider logic to the 100 MHz clock signal generated by the Zed-board clock oscillator.

The output of the transmitter module is given out from one of the I/O pins of the Zed board. This pin is connected to the receiving pin of the UART module connected to the COM port of the PC.

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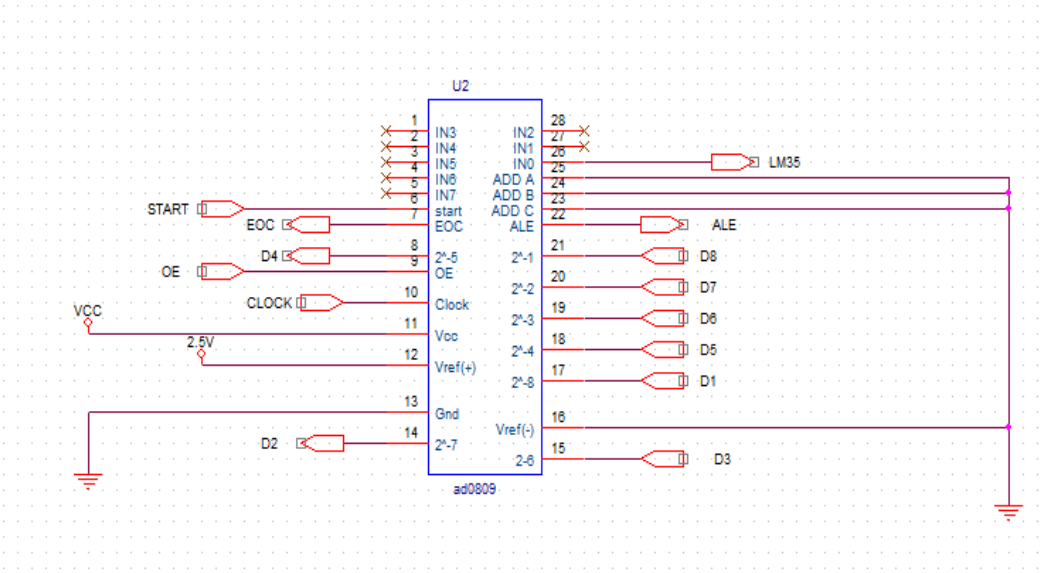

Fig. 6 PCB schematic diagram

V. RESULTS AND DISCUSSIONS

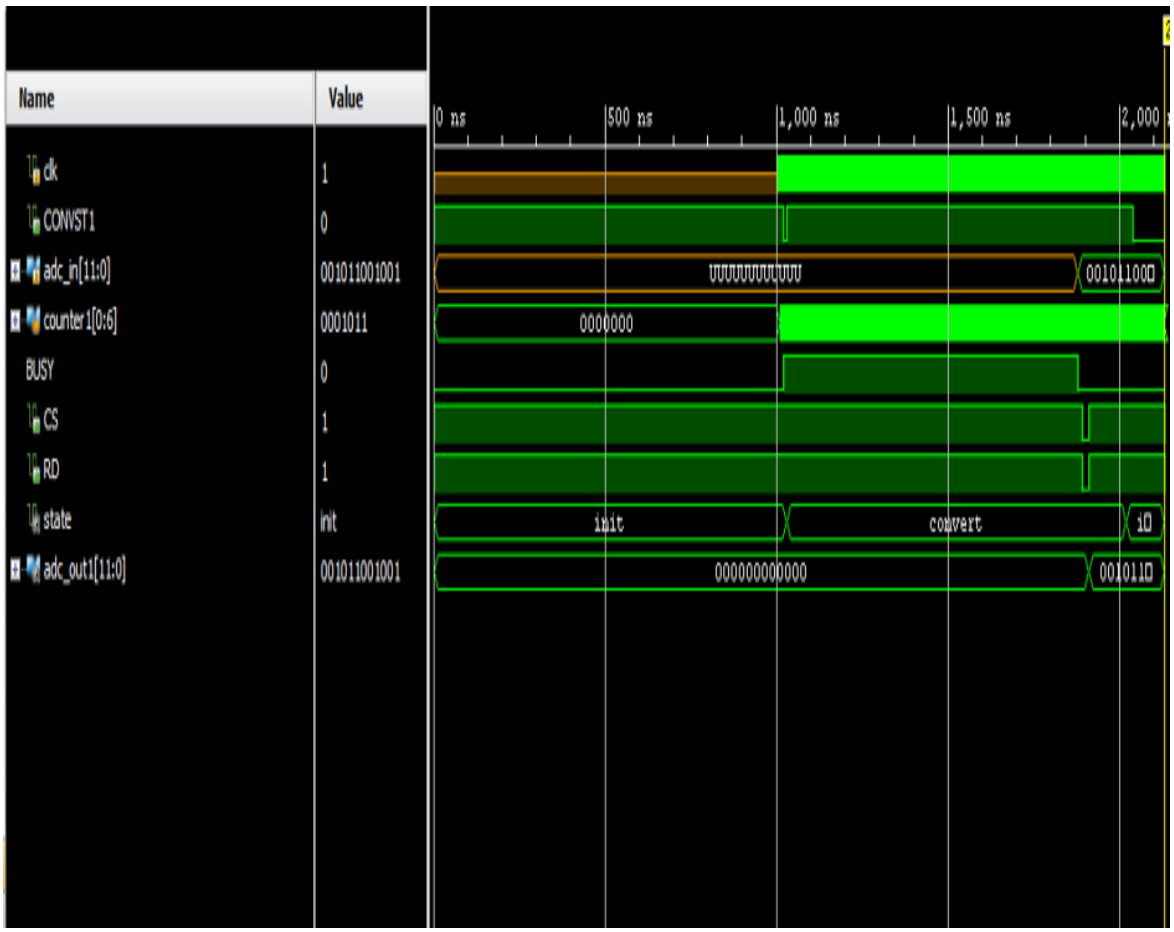

Fig. 7 Behavioural Simulation for FPGA interface for AD7492

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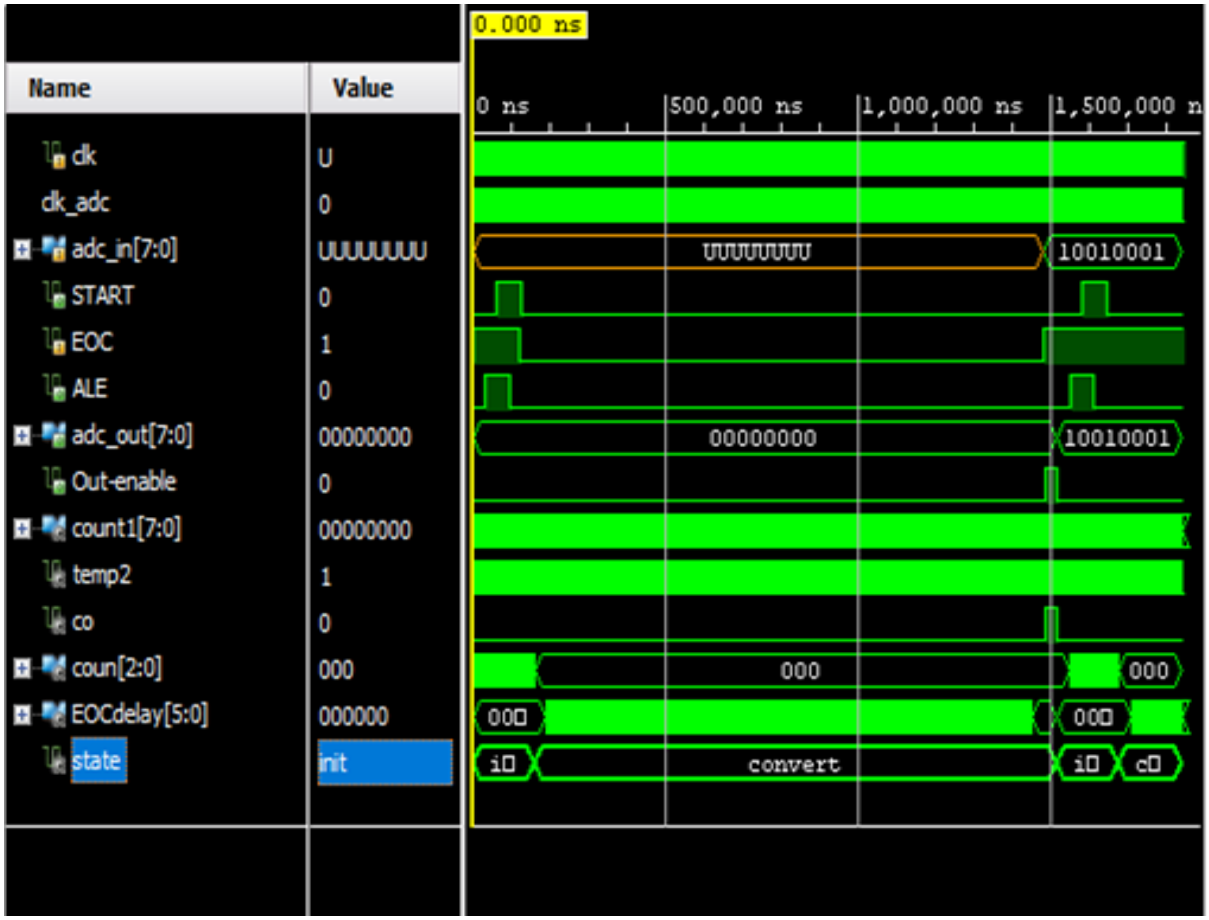

Fig. 8 Behavioural Simulation for FPGA interface for ADC0809

Fig. 7 and Fig. 8 show simulation of interfacing for 12-bit resolution AD7492 and 8-bit resolution AD0809. The simulation results match accurately with the timing diagrams of AD7492 and ADC0809 in [7] and [8] as the logic has been designed such that the pulse width and delay of the signals sent from FPGA for each conversion cycle can be maintained according to the timing specifications mentioned in datasheets [7] [8] because reception of these control signals at wrong time instances can disrupt working of A/D converter. Therefore, the signals are made to change their polarity either at specified counter values or by monitoring response signal (BUSY or EOC) from A/D converter.

It can be seen in Fig. 7 and Fig. 8 that on forcing an input signal 'EOC' and 'Busy', the state gets changed to 'convert'. Again, when the polarity of the 'EOC' and 'Busy' signal is changed the 'Output Enable' signal and 'RD' signals are given out according to the logic discussed in section II.

In hardware implementation the result from A/D converter will be an 8-bit binary number, which has been converted into its BCD equivalent for the convenience of reading and is passed into the hold register of the transmitter. In order to check the data that has been received in the Zed board is getting transmitted serially to PC in correct order using transmitter logic the data is also mapped to the Zed board LEDs.

The result of the hardware implementation on LEDs is shown in Fig. 10 as BCD "0011 0010" which means the temperature of 32℃ is sensed by the LM35 sensor, since the Tera Term software displays the data coming from emulated serial port in ASCII therefore the BCD result sent through transmitter is displayed as ASCII '2' on computer screen as shown in Fig. 9.

Table II shows the resource utilization report generated in the VIVADO software tool.

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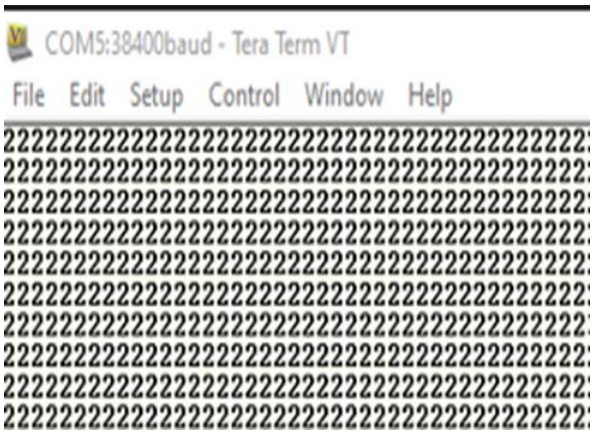

Fig. 9 ASCII equivalent of 32℃

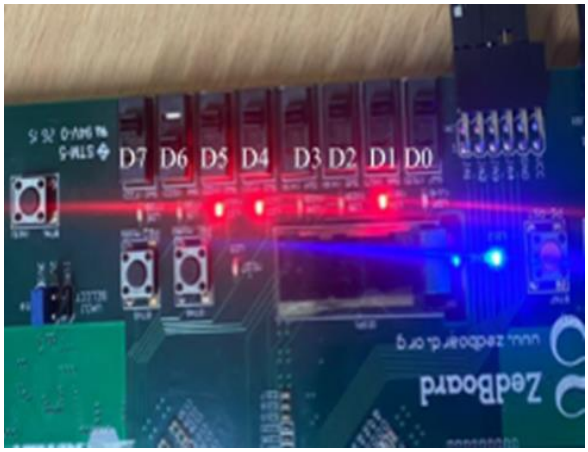

Fig. 10 BCD equivalent to 32℃

TABLE II FPGA SOURCE UTILIZATION CHART

Resource	Utilization	Available	Utilization %
Slice LUTs	141	53200	0.27
Slice Registers	181	106400	0.17
IO	25	202	12.38
Clocking	1	32	3.12

VI. CONCLUSION

The simulation and hardware implementation test done using the proposed methods for interfacing and data transmission show successful results. The simulations run on VIVADO design suite completely matches with the required timing diagrams of both A/D converters.

The hardware implementation shows that ADC0809 accurately converts the acquired sensor data and the transmitter module of UART transmits the data perfectly. The hardware implementation setup can also be used for higher resolution A/D converters such as 12,16. The data can be transmitted through the transmitter module by dividing it into two bytes, sending least significant byte first and then most significant bytes in case of 16-bit resolution A/D converter. In case of 12-bit resolution, data can be sent by either dividing it into two 6-bit chunks or treating 12-bit data as 16 bits by padding zeros in the most significant byte.

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