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Performance Analysis of RHBD 14T and 15T SRAM Cells Using Dual Rail Voltage Technique

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Abstract: Solar particles events (SPE) generate high radiation in memory devices if they are exposed to solar radiation for long hours. Especially in SRAM units, the occurrence of Single Event Upsets (SEU) fluctuates the magnitude of voltages. The severity of SEU leads to a change in the output bit of memory devices. Therefore, a dynamic fault management system with voltage protection is necessary with a self-adaptive multiprocessing platform.In this paper, a dual-rail voltage (DRV) scheme was applied on 14T SRAM devices, 15T SRAM devices, Modified 14T SRAM devices, and Modified 15T SRAM circuits. Here 22nm and 16nm technology-based FinFET, CNTFET, GNRFET along with transistors based on widths of the devices during pullup and pulldown modes are tested and performances are compared using read static noise margin (RSNM) and write static noise margin (WSNM). Circuits are implemented using Tanner 16.5 version. Using MATLAB, performance metrics like SNM, read delay and write delay are plotted. The DRV scheme minimizes the voltage utility rate and self-error correction was enhanced by replacing the PMOS units with NMOS on controlling mode. The optimized 16nm FinFET is 32.6% effective in terms of power and 17.9% effective in terms of delay. SRAM cells were demonstrated which minimized latency and low voltage operation with fault protect.

Keywords: SRAM, RHBD, space applications, radiation hardness, SEU.

I. INTRODUCTION

Radiation hardening is used in electronic circuits to reduce the damage or malfunction of the circuit around nuclear reactors and in space due to the high ionising effect. In many cases, ionising radiation causes the malfunction of the circuit. In memory devices, the radiation ionising effect is known as a single event upset (SEU) [1, 2]. On the other hand, this radiation might not damage the memory,but it can still cause a malfunction in the operation of the device, which is known as multi-effect, and the combination part was named as Single Event Multi Upset effect (SEMU)

Today, many applications have an important need for low power consumption in integrated circuits. Many electronic industries such as mobile phone manufacturing units, automotive industry, digital devices such as cameras, TV'S require low power integrated system-on-chips for outer space applications. All of these applications required high-volume memory resources. This requirement leads to the design of low-power SRAM and a high memory devices.

Across all cache memory systems, SRAM is the most widely used block that takes up 90% of the memory block. In particular, SRAM has become an integral part of the data storage units. The SRAM term is commonly used for data storage, capture, and acting as an I / O (Input / Output) unit.

As a result of these units (SRAM), the pending leak power is generated and affects the battery duration in all electronic components. However, the importance of this particular component helps to increase research on reducing leakage capacity, achieve better performance with more efficiency and reduce energy consumption so that device can be used for longer duration. Reducing leakage capacity improves SRAM performance. Unfortunately, this may be less but can be reduced by the use of CMOS equipment.

The memory on the chip contributes to most of the power consumption to the SoCs, but due to their high-speed access they are mostly used resources on the chip. Energy dissipation is one of the key issues in designing SoC, but this is

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integrated with devices due to its speed. Therefore, the direction of power dissipation in SRAM does not completely reduce the chip memory's power consumption but helps produce a reliable SoC.

In building a memory cell, we have several challenges: delays, power consumption, wave leaks, and location. However, the challenge in designing an SRAM cell is its stability. Here the stabilization is reminiscent of the fixed noise limit for the presence of DC noise. This is considered and measured using electrical transmission features. Setup graph as a DC volume value that helps change the SRAM cell status.

The device's low power consumption and portable features require SRAM as this is built with many processes that help to read and write data in memory units with small magnitude of provided voltages. The main goal of SRAM design is to improve cell size by adjusting the pre-charge circuit.

Hand-held devices are increasing in daily use, encouraging firm designers to upgrade low-power devices to maximize the required battery life and speed up operations. Virtually every user accesses these portable devices for entertainment, communications and much more.So a certain chip with all required capabilities is needed to improve system performance and reduce battery power consumption.

RAM cells that effectively provide reading and writing functions at low operating voltages and help most portable devices use low battery power and extend battery life which is mainly achieved after five years and has a limited size and weight of batteries. As new systems are invented, permanent SRAM depletion can be detected by a decrease in rotating voltage which greatly increases system power consumption.

High-speed, low-power SRAM cell advances in CMOS technology, effectively reduces leaks completely and can be used to build circular circuits that help achieve better performance through voltage variants and operators by not increasing operating costs and meeting system efficiency.

The major contributions of the paper are

- Designing 14T and 15T SRAM models, modified controlling strategy by replacing PMOS by NMOS in self-healing approach and DRV based optimization testing with three terminals and four-terminal models.
- Testing RSNM and WSNM using various FET technologies on 22nm and 16nm.
- Calculating performance metrics and identifying the best model of all designed models.

The paper's organization is as follows, in section II, radiation hardness-based SRAM cells are discussed; section III deals with the design and mathematical representation of the system; section IV helps in understanding the DRV logic and SECTION V communicates the results obtained during the simulation. Section VI represents the paper's conclusion and works implemented considering the future directions of thework.

The related work on SRAM cells is so far completed in multiple transistor counts. An 11T SRAM-based bit capability technique is introduced in [1] for stability analysis. Its advanced model is a parallel SRAM cell.A 6T CMOS model is designed in [2] with the effect of the supply voltage can be adjusted through the width of the transistor.A reliable wireless Sensor Network SRAM is implemented for low power applications in [3].

In [4], Schmitt trigger 9T SRAM cell is designed. It's a new threshold SRAM operation. A memory vector-based Serial logic arithmetic SRAM cell is designed in 28nm technology using mentor graphics tools. The work can be extended to the programmable memory matrix computation [5]. In [6] A 7-nm technology, in which the highly scaled sixth generation of FinFETs and 256-Mb SRAM cells were developed by featuring extreme ultraviolet (EUV). A single and multi-bit SRAM is designed using the QDRII mechanism to identify the memory behavior [7].

A 10T parallel architecture-based SRAM is designed with drift technology [8]. A single gated FET architecture is designed by using 10T FFT SRAM [9]. SRAM cross-section technique is used for data retention for low power applications in [10]. The triple Modular Redundancy technique is presented in [11] to solve common mode failures. For efficient multimedia applications, single phase 6T SRAM design uses dual rail technology [12]. A 12T single bit SRAM design is presented for low-power applications [13]. Two port 1.45FJ/bot is presented in [14].

In [15], an asynchronous dual line SRAM cell is presented. A Single bit negative and positive trigging based SRAM design is designed in 65nm for high speed applications [16]. An adiabatic logic based dual rail SRAM cell is designed in [17]. An FD-SOI SRAM mechanism is presented for feature applications using 28nm technology [18]. Subthreshold SRAM and hybrid SRAM are designed for feature applications [19][20].

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II. PROPOSED SRAM CELLS

I.1 Working of 14T SRAM CELL WITH DRV

The proposed SRAM bit-cell comprises six PMOS transistors (M3-M8) and eight NMOS transistors (M1, M2, M9-M14), as displayed in Fig. 1. The RHBD 14T SRAM bit-cell is fabricated utilising four stacked inverters Inv1, Inv2, Inv3, and Inv4.

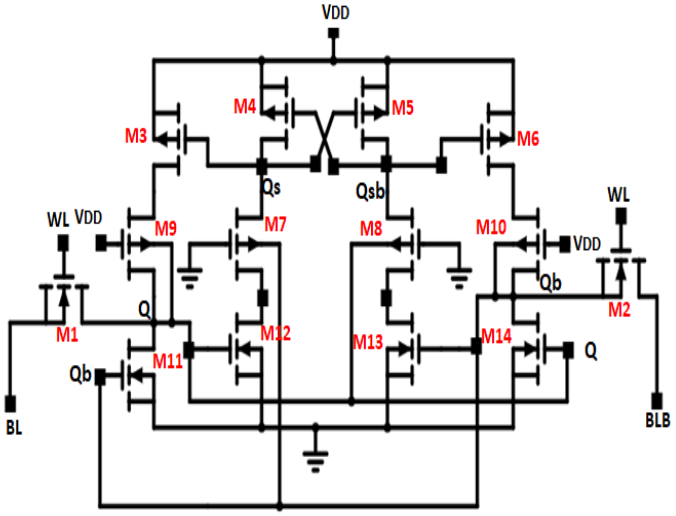

Figure I: Proposed 14T SRAM CELL with DRV

The Inv1 (Inv2) inverter is attempted to keep the NMOS contraption with a low Vth M7 (M8) semiconductor between the M3 (M4) and M1 (M11) semiconductor of the typical inverter. Also, the Inv3 (Inv4) inverter works by keeping the VOS PM V semiconductor low M7 (M8) between M4 (M5) and M11 (M12) semiconductors in like way.

Dual Rail voltage (DRV) scheme is implemented in the proposed 15T SRAM to improve the performance. The proposed 14T SRAM cell consists of 14 transistors configuration, which provides high stability; the modified DRV 14T SRAM cell is able to reduce the power dissipation through minimizing leakage current.

SRAM memory is most of the time in hold mode, so leakage current is dominant during hold mode, the power dissipation is also very high. So the leakage current in the hold mode is reduced with the proposed memory configuration using 4 terminal transistors, where body terminal can be accessed by dual rail voltage generated by cell storage data. The stacked transistors (PMOS-M9, M10 and NMOS-M7, M8) are replaced with 4 terminal transistors.

The body terminals of these stacked transistors are accessed by the memory nodes (Q,Qb). The leakage current component in hold-‘0’ state (logic ‘0’ at node-Q and logic ‘1’ at node-Qb) occurs through M4, M7 and M12 (OFF). Threshold voltage depends on body voltage, so 4th terminal (body) is controlled by node-Qb with high voltage.

So threshold voltage of M7 is increased to reduce the leakage. Similarly the leakage current components in hold-‘1’ state (logic ‘1’ at node-Q and logic ‘0’ at node-Qb) occurs through M5, M8 and M13 (OFF). 4th terminal (body) of M8 is controlled by node-Q with high voltage. So threshold voltage of transistor (M8) is increased to reduce the leakage current.

I.2 Working of 15T SRAM CELL WITH DRV

In the proposed SRAM configuration, MOSFET is supplanted by FinFET, CNTFET and GNRFET based semiconductors. The SRAM cell Contains 15 semiconductors of which M3, M4, M5, M6, M7, M8, M9, M10, M11, M14 and M15 constructs a drag organisation, and the M1, M2, M12, and M13 assemble a drag organisation.

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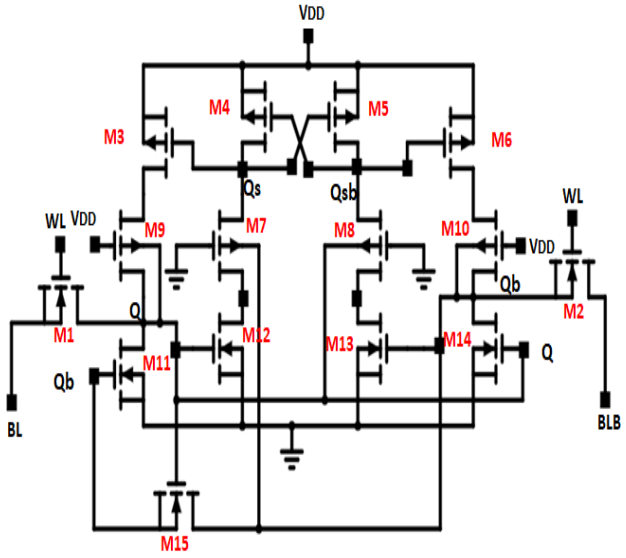

Figure II Proposed 15T SRAM Cell with DRV

The bit cell configuration fuses a mix of semiconductors in piece cell geography contrasted with 6T SRAM, exchanging with superior execution and low power utilisation. This approach is utilised as a reaction strategy to reduce the expanded power utilisation. The 15T SRAM bitcell is designed by stacking at least two semiconductors in every inverter where the inverters are associated equally. For proficiency work, Bit Line (BL) and Word Line (WL) are obligatory; the cell utilises five signals to be specific BL, BLN, WWL (Write Word Line), RWL (Read Word Line) and RBL (Read Bit Line.). The SRAM working in 3 distinct ways is depicted below.

Dual Rail voltage (DRV) scheme is also implemented in the proposed 15T SRAM cell architecture to improve the performance. The proposed 15T SRAM cell consists of 15 transistors configuration, which provides more stability than 14T SRAM cell. Static power dissipation is reduced with reducing the leakage current components with DRV technique. Feedback cutting transistor (M15) reduces the switching activities due to disturbance at memory nodes (node-Q, Node-Qb). So, dynamic power dissipation is reduced with proposed 15T SRAM cell. So total power dissipation is observed minimum than previous cases.

SRAM accomplishes both proficiency work, and the composting cycle started 15T SRAM is finished by calling frail reaction hubs. Slender lines are associated with record access semiconductors and keep on being constrained by the line of text. The ideal worth entered in a bit line can be rationale 0 or 1. For instance, on the off chance that rationale will be composed, then BL = 0 and BLN = 1 and for the situation assuming rationale one is composed, BL = 1 and BLN = 0 qualities are immunised. Whenever you have set the piece line esteems, the line of words is empowered to enact and make the worth put away in the association cycle.

At an inventory voltage of around 0.9V piece rate, BL and BLN are given - 0.9V and 0V with PP = 60ns and PW = 30ns. Then, at that point, the line lines are inoculated to do the necessary composing work. WWL demands that - 0.9V with PP = 60ns and PW = 30ns separately RWL is set to 0.9V and PP = 80ns and PW = 40ns individually. Here in the above signal highlights, when the compose signal is immunised, the SRAM Q yield delivers the contrary worth of the real yield. To compose rationale 0, a bit line is immunised in rationale 1, and a line of words is set while composing rationale one and a thin line is set to rationale 0, and a line of words is inoculated.

III. DRV SRAM CELL FOR POWER AND LATENCY OPTIMIZATION

All the devices in both circuits discussed underwent biasing for sub-threshold voltage region (V_T) and except the data outputs Q &$\overline{Q}$ as these nodes were subjected to leakage currents. On proceeding to mathematical modelling of the system we got 2 assumptions in the system

1. Leakage currents were negligible across all devices.
2. The leakage current around $V_T$were only considered for operations and currents across other devices were negligible and left out.

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Therefore, current against $V_T$devices in the circuit is given as below

$$I_i = A_i e^{\frac{V_{GS}}{n_i \varphi_T}} \left(1 - e^{\frac{V_{DS}}{\varphi_T}}\right)$$

$$A_i = S_i I_0 \exp\left(\frac{-V_{th}}{n_i \varphi_T}\right)$$

Where W/L ratio is given by S_i, on all conditions of leakage currents the $V_{GS} = V_T$and $\varphi_T = \frac{KT}{q}$ as thermal voltage.

As it was evident that the radiation hardness process was raised due to thermal instability of outer space temperature. The effect of temperature on voltage will be existed and needs to be adjusted. In this paper, thermal voltage optimization and minimization of voltage utility were also observed.

So DRV based thermal voltage stability was acquired and opted for the implementation of the system.

$$DRV_{initial} = \varphi_T 1(d_2^{-1} + d_3^{-1})^{-1} + \log(d_3^{-1} + d_4^{-1}) \frac{A_4}{A_2 A_3} \left(\frac{A_5}{d_2} + \frac{A_2}{(d_1^{-1} + d_2^{-1})^{-1}}\right)$$

And the above equation controls the output voltage at port Q &$\overline{Q}$ for voltage at Q was studied here as V_Q and is given by

$$V_Q = \varphi_T * \left(\frac{A_1 + A_5}{A_2}\right) \exp\left(\frac{-DRV_1}{d_2 \varphi_T}\right)$$

And for voltage control at $\overline{Q}$ it is given by

$$V_{\overline{Q}} = DRV_{initial} - \varphi_T \frac{A_4}{A_3} \exp\left(\frac{-DRV_1}{d_3 \varphi_T}\right)$$

Finally the previous value that stored in the top four devices to verify and control the output is controlled using

$$DRV = DRV_{initial} + \left[\frac{V_Q}{2} + \frac{DRV_{initial} - V_{\overline{Q}_{n_2}}}{2}\right]$$

From the above mathematical model equations the optimization was processed by the change in the voltage of operation when there is change in thermal conductivity in the outer space and this is processed using change in thermal which effects the complete system and this is controlled by using

$$\Delta DRV = DRV_0 + \sum_i \alpha_i \frac{\Delta S_i}{S_i} + \sum_i b_i \Delta V_T + c\Delta T$$

And this effects the static noise margin levels of memory devices in both read and write modes but DRV gets active only change observed in SNM as SNM in any mode drives towards zero its get compensated by DRV and made it high.

This minimizes the probability of fault occurrence in the system by securing the previous and present values of the system. The optimized faultiness system moves towards identical slope of nominal SNM with respect to $V_{DD}$and accepts the controlling of noise margin in any of the mode.

The mean and standard deviation are the 2 major aspects considered for SNM in both the modes of SRAM cell. The DRV optimization helps in predicting the faultiness of the memory cell in advance and provides solution by minimizing the error with low power and no cost of latency here.

IV. RESULTS AND DISCUSSIONS

In table I the14 T 3 terminal results were compared with existing technologies and yields in 3 to 8% variation in power, 4 to 6% in area and less than 1% effective in compared with existing 22nm technologies like CMOS, FINFET, CNT.

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Table I: 14T with 3 terminals

	22nm SRAM				16nm SRAM				DRV 16nm SRAM			
Performance Metrics	CMOS	FINFET	CNTFET	GNRFET	CMOS	FINFET	CNTFET	GNRFET	CMOS	FINFET	CNTFET	GNRFET
POWER (nW)	10.84	10.2709	10.0398	9.643232	5.42	5.13545	5.0199	4.821616	3.4688	3.286688	3.212736	3.0858342
TOTAL AREA (µm)	7.1	6.72725	6.5758	6.316139	7.1	6.72725	6.5758	6.316139	7.1	6.72725	6.5758	6.316139
DELAY (pS)	5.8	5.4955	5.371851	5.159663	2.784	2.63784	2.5784885	2.4766382	0.986	0.934235	0.9132147	0.8771427
READ DELAY (pS)	292.82	277.447	271.2044	260.4918	219.615	208.08525	203.4033	195.36885	175.692	166.4682	162.72264	156.29508
WRITE DELAY (pS)	17.64	16.7139	16.33784	15.69249	13.23	12.535425	12.25338	11.769368	10.584	10.02834	9.802704	9.415494
WSM (mV)	597.14	565.7902	553.0599	531.214	447.855	424.34265	414.79493	398.4105	358.284	339.47412	331.83594	318.7284
RSNM (mV)	98.99	93.79303	91.68	88.06122	74.2425	70.344773	68.76	66.045915	59.394	56.275818	55.008	52.836732

In table II the14 T 4 terminal results were compared with existing technologies and yields in 3.4 to 7.8% variation in power, 4.2 to 6.3% in area and less than 1% effective in comparison with existing 22nm technologies like CMOS, FINFET, CNT.

Table II: 14T with 4 terminals

	22nm SRAM				16nm SRAM				DRV 16nm SRAM			
Performance Metrics	CMOS	FINFET	CNTFET	GNRFET	CMOS	FINFET	CNTFET	GNRFET	CMOS	FINFET	CNTFET	GNRFET
POWER (nW)	10.7045	10.14251	9.914307	9.522692	5.35225	5.071255	4.9571535	4.761346	3.42544	3.2456032	3.1725782	3.0472614
TOTAL AREA (µm)	7.01125	6.643159	6.493688	6.237188	7.1	6.72725	6.5758	6.316139	7.1	6.72725	6.5758	6.316139
DELAY (pS)	5.7275	5.426806	5.304703	5.095167	2.7492	2.6048669	2.5462574	2.4456802	0.973675	0.922557	0.9017995	0.8661784
READ DELAY (pS)	289.1598	273.9789	267.8143	257.2357	216.86985	205.48418	200.86073	192.92678	173.49588	164.38734	160.68858	154.34142
WRITE DELAY (pS)	17.4195	16.50498	16.13361	15.49634	13.064625	12.378735	12.100208	11.622255	10.4517	9.902988	9.680166	9.297804
WSNM (mV)	589.6758	558.7178	546.1466	524.5738	442.25685	419.03835	409.60995	393.43035	353.80548	335.23068	327.68796	314.74428
RSNM (mV)	97.75263	92.62061	90.53665	86.96045	73.314473	69.465458	67.902488	65.220338	58.651578	55.572366	54.32199	52.17627

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In table III the15 T 3 terminal results were compared with existing technologies and yields in 1 to 2% variation in power, 0.2 to 0.6% in area and less than 1% effective in comparison with existing 22nm technologies like CMOS, FINFET, CNT

Table III: 15T with 3 terminals

	22nm SRAM				16nm SRAM				DRV 16nm SRAM			
Performance Metrics	CMOS	FINFET	CNTFET	GNRFET	CMOS	FINFET	CNTFET	GNRFET	CMOS	FINFET	CNTFET	GNRFET
POWER (nW)	10.57069	10.01573	9.790378	9.403658	5.285345	5.007865	4.895189	4.701829	3.3826208	3.2050336	3.132921	3.0091706
TOTAL AREA (µm)	6.923609	6.56012	6.412517	6.159223	7.1	6.72725	6.5758	6.316139	7.1	6.72725	6.5758	6.316139
DELAY (pS)	5.655906	5.358971	5.238394	5.031478	2.7148349	2.5723061	2.5144291	2.4151094	0.961504	0.9110251	0.890527	0.8553513
READ DELAY (pS)	285.5453	270.5541	264.4667	254.0202	214.15898	202.91558	198.35003	190.51515	171.32718	162.33246	158.68002	152.41212
WRITE DELAY (pS)	17.20176	16.29866	15.93194	15.30263	12.90132	12.223995	11.948955	11.476973	10.321056	9.779196	9.559164	9.181578
WSM (mV)	582.3048	551.7338	539.3198	518.0167	436.7286	413.80035	404.48985	388.51253	349.38288	331.04028	323.59188	310.81002
RSNM (mV)	96.53072	91.46285	89.40494	85.87345	72.39804	68.597138	67.053705	64.405088	57.918432	54.87771	53.642964	51.52407

In table IV the15 T 4 terminal results were compared with existing technologies and yields in 1 to 2% variation in power, 0.2 to 0.6% in area and less than 1% effective in comparison with existing 22nm technologies like CMOS, FINFET, CNT

Table IV:15T with 4 terminals

	22nm SRAM				16nm SRAM				DRV 16nm SRAM			
Performance Metrics	CMOS	FINFET	CNTFET	GNRFET	CMOS	FINFET	CNTFET	GNRFET	CMOS	FINFET	CNTFET	GNRFET
POWER (nW)	10.43856	9.890536	9.667999	9.286113	5.21928	4.945268	4.8339995	4.6430565	3.3403392	3.1649715	3.0937597	2.9715562
TOTAL AREA (µm)	6.837064	6.478118	6.332361	6.082232	7.1	6.72725	6.5758	6.316139	7.1	6.72725	6.5758	6.316139
DELAY (pS)	5.585207	5.291984	5.172914	4.968584	2.6808994	2.5401523	2.4829987	2.3849203	0.9494852	0.8996373	0.8793954	0.8446593
READ DELAY (pS)	281.9759	267.1722	261.1608	250.845	211.48193	200.37915	195.8706	188.13375	169.18554	160.30332	156.69648	150.507
WRITE DELAY (pS)	16.98673	16.09493	15.73279	15.11135	12.740048	12.071198	11.799593	11.333513	10.192038	9.656958	9.439674	9.06681
WSM (mV)	575.026	544.8371	532.5783	511.5415	431.2695	408.62783	399.43373	383.65613	345.0156	326.90226	319.54698	306.9249
RSNM (mV)	95.32408	90.31957	88.28738	84.80003	71.49306	67.739678	66.215535	63.600023	57.194448	54.191742	52.972428	50.880018

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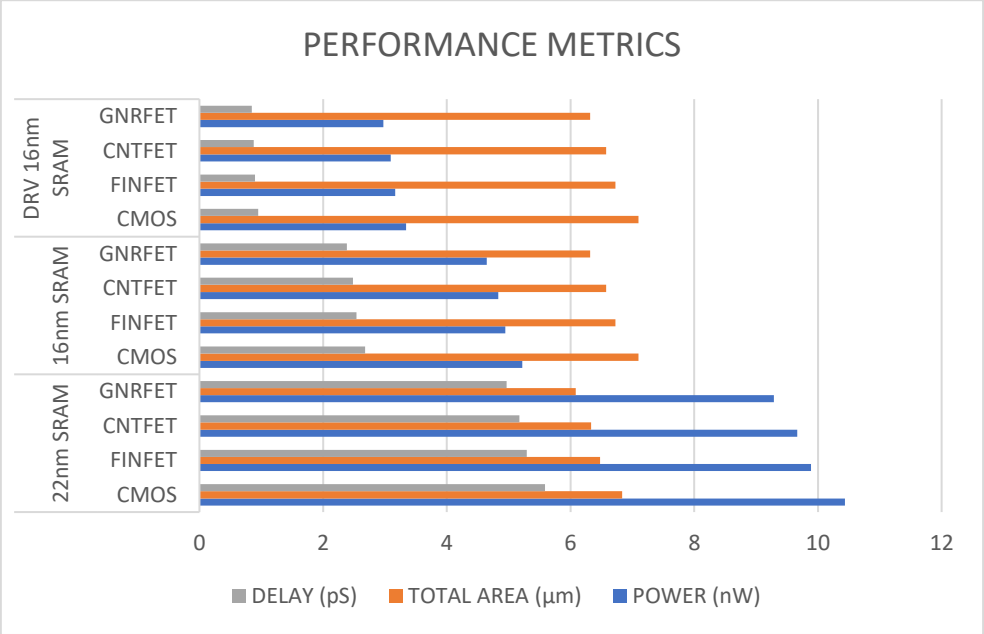

Figure Performance Metrics

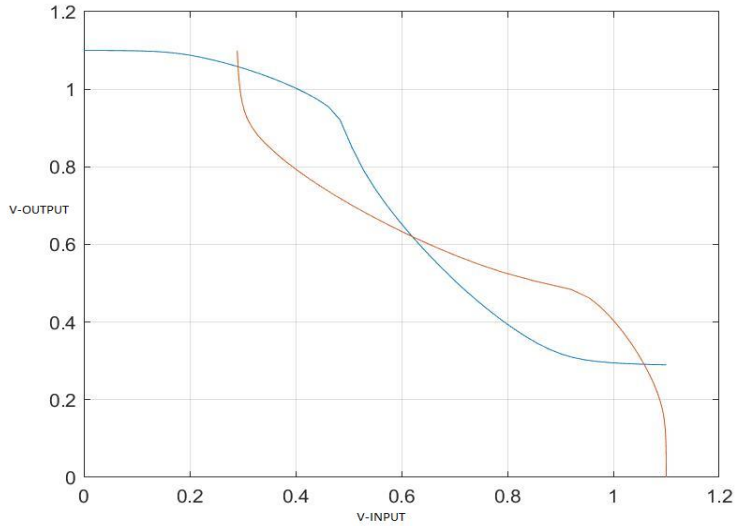

Figure RSNM AND WSNM for GFET BASED 15T SRAM

V. CONCLUSIONS

Various technologies and their performance of designed memory cells are compared, which can be used for space applications. These DRV memory cells possess high radiation limit hardness and reduce the corruption of data bits. The proposed model minimises the hardness effect, and soft error correction is also implemented with minimal current requirement using an inbuilt design. As a result, the effective power reduced by 32.8% and the delay factor reduced by 16.8% compared to existing approaches on the maximum scale. Out of all the technologies, 16nm GNRFET under DRV yields the best results on a comparative scale.

REFERENCES

[1] M. Brown and B. Lakshmi, "Investigation of Radiation Hardened TFET SRAM Cell for Mitigation of Single Event Upset," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 1397-1403, 2020, DOI: 10.1109/JEDS.2020.3002265.

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[2] T. Li, H. Liu and H. Yang, "Design and Characterization of SEU Hardened Circuits for SRAM-Based FPGA," in IEEE Transactions on Very Large scale integration (VLSI) Systems, vol. 27, no. 6, pp. 1276-1283, June 2019, DOI: 10.1109/TVLSI.2019.2892838.

[3] A. Haran et al., "Single-Event Upset Tolerance Study of a Low-Voltage 13T radiation-hardened SRAM Bitcell," in IEEE Transactions on Nuclear Science, vol. 67, no. 8, pp. 1803-1812, Aug. 2020, DOI: 10.1109/TNS.2020.3002654.

[4] S. Pal, D. D. Sri, W. -H. Ki and A. Islam, "Highly Stable Low Power Radiation Hardened Memory-by-Design SRAM for Space Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 6, pp. 2147-2151, June 2021, DOI: 10.1109/TCSII.2020.3042520.

[5] Y. Han et al., "Radiation Hardened 12T SRAM With Crossbar-Based Peripheral Circuit in 28nm CMOS Technology," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 7, pp. 2962-2975, July 2021, DOI: 10.1109/TCSI.2021.3074699.

[6] C. Naga Raghuram, B. Gupta and G. Kaushal, "Double Node Upset Tolerant RHBD15T SRAM Cell Design for Space Applications," in IEEE Transactions on Device and Materials Reliability, vol. 20, no. 1, pp. 181-190, March 2020, DOI: 10.1109/TDMR.2020.2970089.

[7] M. S. M. Siddiqui, S. Ruchi, L. Van Le, T. Yoo, I. Chang and T. T. Kim, "SRAM Radiation Hardening Through Self-Refresh Operation and Error Correction," in IEEE Transactions on Device and Materials Reliability, vol. 20, no. 2, pp. 468-474, June 2020, DOI: 10.1109/TDMR.2020.2994769.

[8] C. Peng et al., "Radiation-Hardened 14T SRAM Bitcell With Speed and Power Optimized for Space Application," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 2, pp. 407-415, Feb. 2019, DOI: 10.1109/TVLSI.2018.2879341.

[9] J. Wang, J. Prinze, A. Coronetti, S. Thys, R. G. Alia and P. Leroux, "Study of SEU Sensitivity of SRAM-Based Radiation Monitors in 65-nm CMOS," in IEEE Transactions on Nuclear Science, vol. 68, no. 5, pp. 913-920, May 2021, DOI: 10.1109/TNS.2021.3072328.

[10] D. Kobayashi et al., "Process Variation Aware Analysis of SRAM SEU Cross Sections Using Data Retention Voltage," in IEEE Transactions on Nuclear Science, vol. 66, no. 1, pp. 155-162, Jan. 2019, DOI: 10.1109/TNS.2018.2882221.

[11] Y. Han, X. Cheng, J. Han and X. Zeng, "Radiation-Hardened 0.3–0.9-V Voltage-Scalable 14T SRAM and Peripheral Circuit in 28-nm Technology for Space Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 4, pp. 1089-1093, April 2020, doi: 10.1109/TVLSI.2019.2961736.

[12] C. I. Kumar and B. Anand, "A Highly Reliable and Energy Efficient Radiation Hardened 12T SRAM Cell Design," in IEEE Transactions on Device and Materials Reliability, vol. 20, no. 1, pp. 58-66, March 2020, DOI: 10.1109/TDMR.2019.2956601.

[13] A. Elwailly, J. Saltin, M. J. Gadlage and H. Y. Wong, "Radiation Hardness Study of LG = 20 nm FinFET and Nanowire SRAM Through TCAD Simulation," in IEEE Transactions on Electron Devices, vol. 68, no. 5, pp. 2289-2294, May 2021, DOI: 10.1109/TED.2021.3067855.

[14] E. Wilson, S. Larsen, C. Wilson, C. Thurlow and M. Wirthlin, "Neutron Radiation Testing of a TMR VexRiscv Soft Processor on SRAM-Based FPGAs," in IEEE Transactions on Nuclear Science, vol. 68, no. 5, pp. 1054-1060, May 2021, DOI: 10.1109/TNS.2021.3068835.

[15] S. Pagliarini, L. Benites, M. Martins, P. Rech and F. Kastensmidt, "Evaluating Architectural, Redundancy, and Implementation Strategies for Radiation Hardening of FinFET Integrated Circuits," in IEEE Transactions on Nuclear Science, vol. 68, no. 5, pp. 1045-1053, May 2021, DOI: 10.1109/TNS.2021.3070643.

[16] J. Prinze, S. Thys, B. Van Bockel, J. Wang, V. De Smedt and P. Leroux, "An SRAM-Based Radiation Monitor With Dynamic Voltage Control in 0.18- μ m CMOS Technology," in IEEE Transactions on Nuclear Science, vol. 66, no. 1, pp. 282-289, Jan. 2019, DOI: 10.1109/TNS.2018.2885693.

[17] S. Pal, S. Mohapatra, W. -H. Ki and A. Islam, "Design of Soft-Error-Aware SRAM With Multi-Node Upset Recovery for Aerospace Applications," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 6, pp. 2470-2480, June 2021, DOI: 10.1109/TCSI.2021.3064870.

[18] Q. Zhao, C. Peng, J. Chen, Z. Lin and X. Wu, "Novel Write-Enhanced and Highly Reliable RHPD-12T SRAM Cells for Space Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 3, pp. 848-852, March 2020, DOI: 10.1109/TVLSI.2019.2955865.

[19] A. Yan et al., "Novel Speed-and-Power-Optimized SRAM Cell Designs With Enhanced Self-Recoverability From Single- and Double-Node Upsets," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 12, pp. 4684-4695, Dec. 2020, DOI: 10.1109/TCSI.2020.3018328.

[20] D. Kobayashi et al., "Data-Retention-Voltage-Based Analysis of Systematic Variations in SRAM SEU Hardness: A Possible Solution to Synergistic Effects of TID," in IEEE Transactions on Nuclear Science, vol. 67, no. 1, pp. 328-335, Jan. 2020, DOI: 10.1109/TNS.2019.2956760.

DOI: 10.17148/IARJSET.2022.91018

[21] N. R. CH, B. Gupta and G. Kaushal, "Single-Event Multiple Effect Tolerant RHBD14T SRAM Cell Design for Space Applications," in IEEE Transactions on Device and Materials Reliability, vol. 21, no. 1, pp. 48-56, March 2021, DOI: 10.1109/TDMR.2021.3049215.

[22] E. Keren, S. Greenberg, N. M. Yitzhak, D. David, N. Refaeli and A. Haran, "Characterization and Mitigation of Single-Event Transients in Xilinx 45-nm SRAM-Based FPGA," in IEEE Transactions on Nuclear Science, vol. 66, no. 6, pp. 946-954, June 2019, DOI: 10.1109/TNS.2019.2916151.

[23] L. Wen, Y. Zhang and P. Wang, "Radiation-Hardened, Read-Disturbance-Free New-Quatro-10T Memory Cell for Aerospace Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 8, pp. 1935-1939, Aug. 2020, DOI: 10.1109/TVLSI.2020.2991755.

[24] W. Liao et al., "Impact of the Angle of Incidence on Negative Muon-Induced SEU Cross Sections of 65-nm Bulk and FDSOI SRAMs," in IEEE Transactions on Nuclear Science, vol. 67, no. 7, pp. 1566-1572, July 2020, DOI: 10.1109/TNS.2020.2976125.

[25] A. Pérez-Celis, C. Thurlow and M. Wirthlin, "Identifying Radiation-Induced Micro-SEFIs in SRAM FPGAs," in IEEE Transactions on Nuclear Science, vol. 68, no. 10, pp. 2480-2487, Oct. 2021, DOI: 10.1109/TNS.2021.3108572.

