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Design and Simulation of 4 bit- Successive Approximation ADC

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Abstract: The digital signal is easy to process than the analog circuits. The design of digital circuits is less complex than the analog circuit. The digital circuit is cheap, robust, stable, less affected by noise and more accurate than analog circuit. The analog to digital converter is bridge between digital and analog. The biomedical and industrial sensor requires powerful analog to digital converter which consume less energy and high speed of operation.

In this paper, the four-bit successive approximation ADC is designed which consumes less power with high precision. The converter consists of SAR (Successive Approximation Register), Weighted Register Digital to analog converter and comparator. The simulation of the circuit is implemented and tested into proteus software.

Keywords: Analog to Digital Converter, Successive Approximation Register, simulation.

I. INTRODUCTION

Successive Approximation type ADC is the most widely used and popular ADC method. The successive approximation ADC used in biomedical, industrial circuits, Voltmeters, ammeters, multimeter etc.

The successive approximation ADC is used to approximate the given analog input with higher accuracy, low power and in less time. ADC plays an important role where there is need of increasing digital components these demand increases in industrial equipment's, biomedical and sensors which demand low power consumption, accurate and more life. The technologies like VLSI make the device compact. The ADC is used where the accuracy is needed. The accuracy of the ADC depends upon the resolution. While the error of the ADC varies on its linearity. ADC plays in important role where accuracy is needed. The most popular ADC is the flash ADC but it consumes much power because of the many comparators.

II. LITERATURE REVIEW

ADC plays an important role in many processing circuits. In all the different types the Successive Approximation ADC is used where the low power, high resolution is required. The recent development in the field of CMOS ADC decreases the power consumption and increase the efficiency. The ADC have accurate for low to medium resolution. In some research time complexity is decreased based on the design. The capacitance plays important role for deciding the time complexity and power consumption. The number of capacitance decrease switching and power consumption.

In this proposed paper the time and power consumption by the design so it can solve the problem based on the need of the biomedical devices.

Architecture:

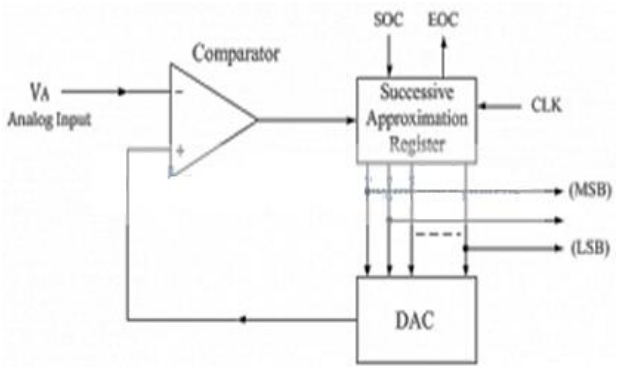

Fig: Typical Block of DAC

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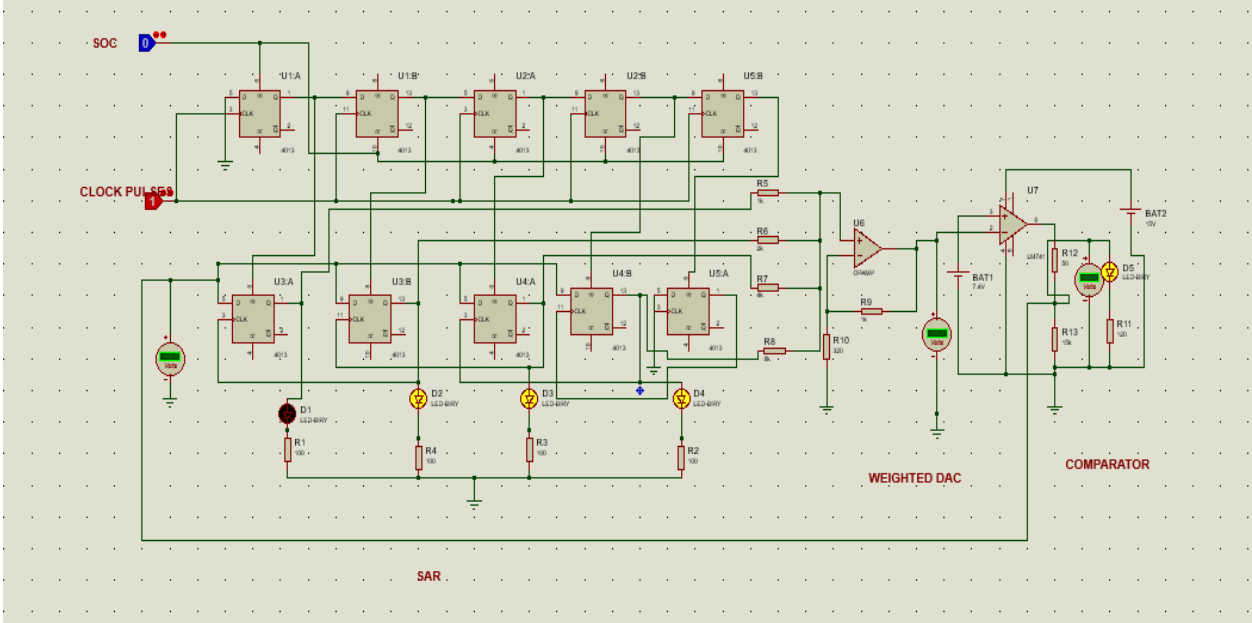

When the start command is applied, the SAR sets the MSB to logic 1 and other bits are made logic 0, so that the trial code becomes 1000.

This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps.

(1) The MSB is initially set to 1 with the remaining three bits set as 0000. The digital equivalent voltage is compared with the unknown analog input voltage.
(2) If the analog input voltage is higher than the digital equivalent voltage, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to 0 and the second MSB is set to 1. Comparison is made as given in step (1) to decide whether to retain or reset the second MSB.

The above steps are more accurately illustrated with the help of an example.

Let us assume that the 4-bit ADC is used and the analog input voltage is VA = 11 V. when the conversion starts, the MSB bit is set to 1.

Now VA = 11V > VD = 8V = [1000]2

Since the unknown analog input voltage VA is higher than the equivalent digital voltage VD, as discussed in step (2), the MSB is retained as 1 and the next MSB bit is set to 1 as follows

VD = 12V = $[1100]_2$
Now VA = 11V < VD = 12V = $[1100]_2$

Here now, the unknown analog input voltage VA is lower than the equivalent digital voltage VD. As discussed in step (2), the second MSB is set to 0 and next MSB set to 1 as

VD = 10V = $[1010]_2$
Now again VA = 11V > VD = 10V = $[1010]_2$

Again, as discussed in step (2) VA>VD, hence the third MSB is retained to 1 and the last bit is set to 1. The new code word is

VD = 11V = $[1011]_2$
Now finally VA = VD , and the conversion stops.

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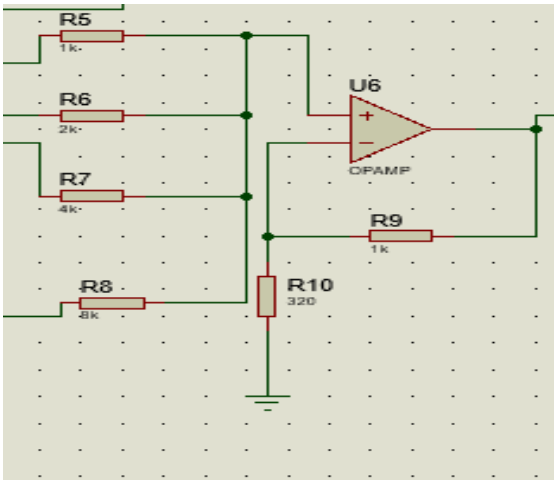
Hardware

1) WEIGHTED DAC:

A weighted DAC produces an analog output, which is almost equal to the digital input by using binary weighted resistor in non-inverting adder circuit. The resistor 1k, 2k, 4k and 8k is given to the non-inverting input of the op-amp whereas the feedback resistor is connected to the inverting input.



Since the number of inputs is four in the binary input, we will get sixteen possible value of output voltage by varying the binary input 0000 to 1111 for a fixed reference voltage V_R.
Output of DAC is applied to the inverting input of the comparator.

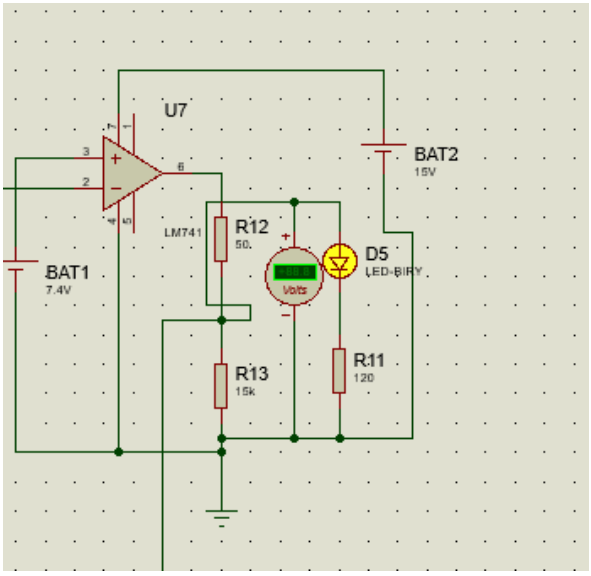
2) Comparator:

Comparator compare the the two inputs voltage and output a binary signal indicating which is larger.

If the non-inverting input is grater than the inverting input, the output goes high. If the inverting input is grater than the non-inverting the output goes low.

Due to high open loop gain, the output of the comparator is +Vcc or -Vcc.

The voltage comparator is 1 bit analog to digital converter as the input signal is analogue but the output behaves digitally. The output of the comparator is connected to the SAR.



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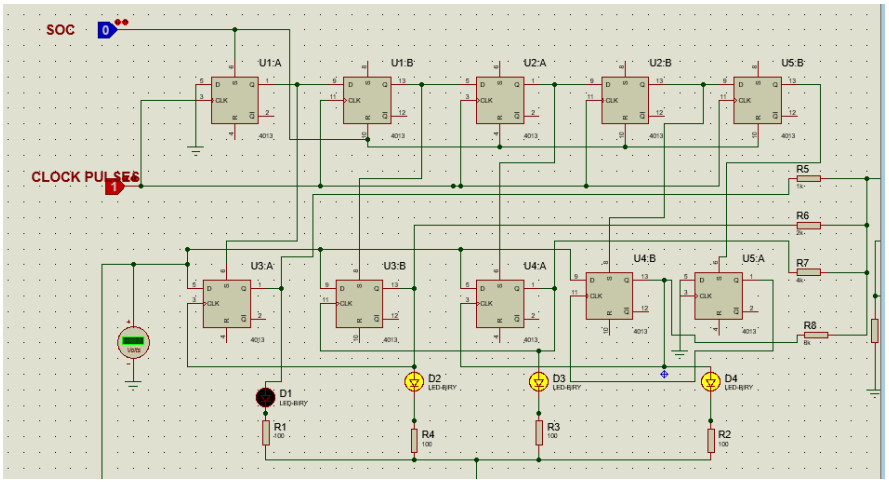
3) SAR (Successive approximation ADC)



SAR consist of ring counter which is divided into control logic and comparator. The SAR consists of D flip flops. Control logic is depended upon the output from the comparator. According to the output of the comparator, the shift register decides whether to shift the output of the ring counter. The SAR works on asynchronous clock. As the output from the previous flip flop act clock input to the next flip flop. This method was proposed by Anderson. The SAR starts by the SOC (start of the conversion). The output of the SAR is given to the input of ADC. The circuit is reset by the reset input. The circuit works like binary search. One can add more shift register to the circuit and extend the circuit to implement the algorithm. The increase in shift register increases the power consumption and propagation delay. The clock is given manually but it can be processed using the clock generator.

III. CONCLUSION

SAR ADC is the most efficient ADC, this is because of its Power Efficiency, Complexity, Conversion rate which is better than the flash ADC, single and dual slope ADC. This paper gives architecture of the ADC which is Comparator, DAC and SAR. Along with the binary search algorithm, the parameter like offset error, gain error, parasitic effect, jitter and management all these considered while designing the circuit. It is observed that the ADC have conversion time of less than 100 micro sec with less power consumption.

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