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IMPLEMENTATION OF BROKAW BANDGAP REFERENCE

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Abstract: In this study, a high-performance CMOS band-gap reference (BGR) is designed. The suggested circuit uses a current mode architecture that has been specially designed for low supply voltage situations. The main component of the circuit uses the Brokaw BGR architecture, which only uses first-order temperature compensation technology and a three-stage operational amplifier to achieve high PSRR and a low temperature coefficient. The circuit uses Chartered 0.18-m CMOS technology and operates at 1.8 volts, simulation results are provided. According to the simulation's findings, the temperature coefficient is 9 ppm/K for the -40 to 125°C temperature range, and the reference voltage fluctuates by no more than 0.067 mV when the power voltage shifts from 1.44 to 2.16V. The PSRR is 108.5dB at 10 KHz with the power consumption of only 0.355mW as well.

Keywords: PMOS, NMOS, Low power applications, Constant Voltage, RLC Circuits, PSRR, Stability Analysis, Noise Parameters.

I. INTRODUCTION

Different topologies have been compared, includi ng resistor-terminated, resistive feedback, current reuse, commongate, and source inductive degeneration. Although gain is improved by 10% using dual CS transistors with inductive degeneration, wideband gain flatness is not present. Similar to how current reuse increases the linearity of the circuit with low noise figure but has stability difficulties, common gate architecture delivers flat gain with improved linearity but higher noise figures. In order to create dual band circuits and get the appropriate LNA parameters, two stagecircuits integrating two different topologies are used. As a result, the main focus of this study is to develop a single-stage,single-band LNA with low noise and high gain, which is still an issue in earlier studies because the noise figure obtained is more than 2 dB. In keeping with this, four distinct cascade topologies for 2.8GHz center frequency using 180nm RF CMOS technology have been implemented in ADS Software. Based on the performance of these LNAs, a unique circuit has been developed that offers the greatest results in terms of gain, noise figure, and stability. The inter stage LC circuit, best impedance matching networks, and current reuse technology are mostly used to reduce noise figure with greater gain. This method lowers noise at the input stage while increasing input impedance. The following describes the structure of this essay. Four distinct cascode topologies are included in Section 2's discussion of the fundamental LNA topologies. This design offers low noise figure at low frequencies, but as the frequencies increase, it increases, which becomes a problem. The relevance of a low-noise amplifier in radio reception circuits cannot be overstated.

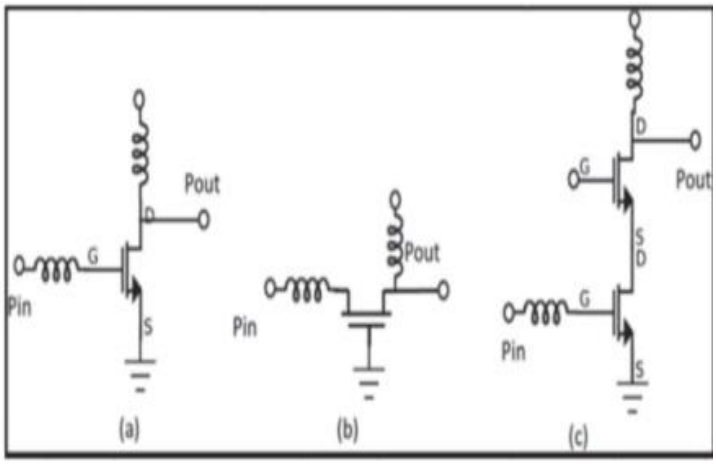

Fig. 1 Basic three topologies

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The relevance of a low-noise amplifier in radio reception circuits cannot be overstated. LNA must offer high-gain, low-noise figure, and superior input and output matching, and strong linearity as a crucial component of the receiver. Figure 1's fundamental three topologies explain how to configure devices correctly.

In Figure 1(a), the Common Source (CS) topology offers low noise, but at the expense of greater sensitivity to process change, temperature, and power supply. This architecture has a stability problem because it frequently needs to be compensated. Better input impedance is the primary goal of the Common Gate (CG) topology. A cascoded common-source amplifier, a folded cascode amplifier, and a shunt feedback amplifier are the three low-noise amplifier topologies that are implemented.

II. LITERATURE SURVEY

Y.-T. Ku, and S.-F. Wang described a novel wide-band low-voltage LNA for CMOS is developed [1]. The suggested LNA uses gain enhanced and negative feedback to boost its high-frequency gain and concurrently attain high gain and wide bandwidth. To achieve full output swing, the suggested LNA employs a mirror bias approach, and its operational current is unaffected by variations in the supply voltage. The gain flatness, high gain, and low noise figure can all be enhanced by the two-stage architecture. As a result, the designed LNA has superior gain flatness performance, low noise, high gain, and wide bandwidth. The proposed LNA's operating bandwidth ranges from 1.5 to 3.5 GHz and The proposed LNA's noise figure is less than 4.2 dB, its measured gain is higher than 15 dB, its measured input third-order intercept points (IIP3) are -7 dBm, and its measured power dissipation at 1 V supply voltage is 8 mW. The proposed LNA is put into practice using a 0.18-m RF CMOS technology in a 0.28 mm2 chip area.

B. Prameela, and A. E. Daniel protocol, WLAN, this study compares the performance of two Low Noise Amplifiers (LNA), a basic Cascode and a modified Cascode LNA. The performance metrics of a modified cascode LNA with dual Common source transistors are compared to those of a simple cascode stage [2]. At 2.4 GHz and a supply voltage of 1.8V, the improved cascode stage has a high gain of 19.2dB and an optimum noise figure of 0.416dB. S11: -13.74 dB; S22: -0.87 dB; S12: -43.63 dB. IIP3 is -8.42dBm and P1dB is -18.35dBm. Over a range of 2-3 GHz, the LNA is intended to be steady. The circuit consumes 8.1 mW of power. Andrew Roobert, and D. Gracia Nirmala Rani describe a dual-band complementary metal-oxide-semiconductor (CMOS) LNA for 2G, 3G, and 4G mobile communications. It uses frequencies of 0.9 and 2.3 GHz. By using a modified notch-filtering path in the wideband LNA, the dual-band functioning is made possible. To cancel the signals of the stop band frequency, the updated notch-filtering path doesn't need any more power. The proposed LNA's filtering path's effect is examined. In dual frequency bands, betteroutcomes are seen. Examined for sustainability under process corner and temperature variation, the LNA is determined to be appropriate for the application.

A. Hashim, N. M. Noh, S. K. KunhiMohd, Y. Mohd Yusof, M. Haidar Hamzah, M [3] This research focuses on the design of a fully integrated PCSNIM LNA, a 0.13-m CMOS multi-standard low-noise amplifier with power constraints. CMOS switches are used to implement the multi-standard capabilities. When compared to the current multi-standard LNA topologies, this approach is unusual in that the input and output matching are entirely implemented on a chip. Operating at frequencies of 0.9, 1.8, and 2.1 GHz is the multi-standard LNA. The design included wireless applications using the GSM900, DCS1800, and W-CDMA protocols.

J Linxiao Shen; Nanshu Lu; Nan Sun [4] A very power-efficient amplifier is shown in this study. The suggested amplifier achieves six-time current reuse by stacking inverters and dividing the capacitor feedback network, considerably enhancing the trans conductance and decreasing noise without increasing current consumption. In order to provide reliable operation under a 1-V supply, a unique biasing mechanism is developed. A 180-nm CMOS prototype has the best noise efficiency factor of 1.07 among known amplifiers with 5.5-V rms noise within 10-kHz BW while using only 0.25-W of power.

III. METHODOLOGY

To create a current that is proportional to absolute temperature (PTAT) in a resistor, two p-n junctions (such as diodes) are operated at differing current densities. A second resistor receives a voltage from this current in order to operate. This voltage is then added to the voltage of one junction (or, in certain systems, a third one). Complementary to absolute temperature (CTAT) is the relationship between the voltage across a diode operating at constant current and the temperature, with a temperature coefficient of roughly 2 mV/K. The first order effects of the diode's temperature sensitivity and the PTAT current will cancel out if the ratio between the first and second resistors is suitably set.

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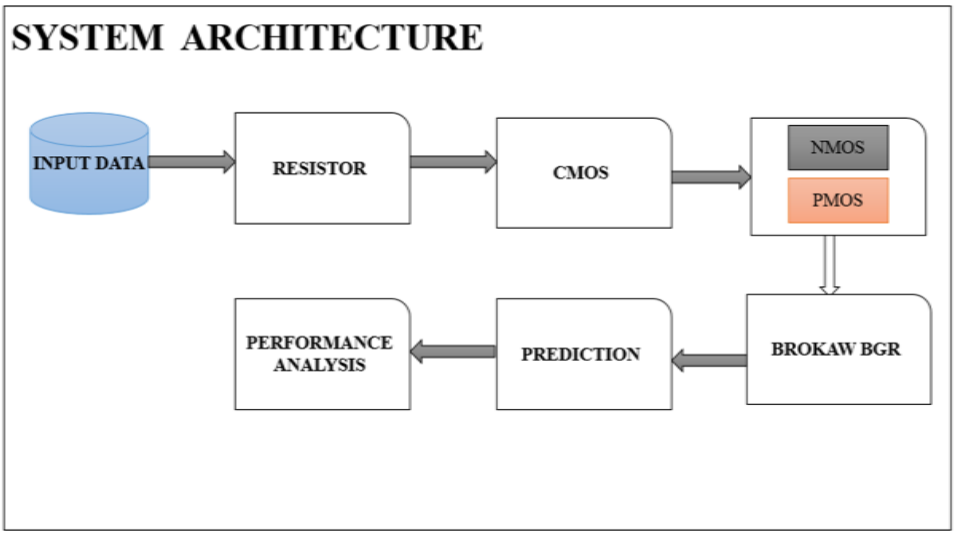

Fig. 2 BGR block diagram

Power efficiency and circuit size are the other important factors to consider while designing bandgap references. A bandgap reference is typically relied on BJT components and resistors, so the overall circuit size may be substantial and consequently costly for IC design. Additionally, this form of circuit may use a lot of energy to meet the required noise and precision specifications. Bandgap references (BGRs) are frequently employed to produce a temperature-insensitive reference voltage based on the bandgap of silicon. The BGR typically uses PN diodes to provide both proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) numbers, combining them to remove the temperature dependence. Though using a reliable voltage or current reference that is insensitive to preferable to CMOS-only in terms of process, voltage, and temperature fluctuations. Reference circuits, it hasn't gotten much consideration in ultra-low-power (ULP) sensor technology applications.

Types of modules:

- Input Data
- Resistor
- CMOS
- BROKAW BGR
- Prediction
- Result generation

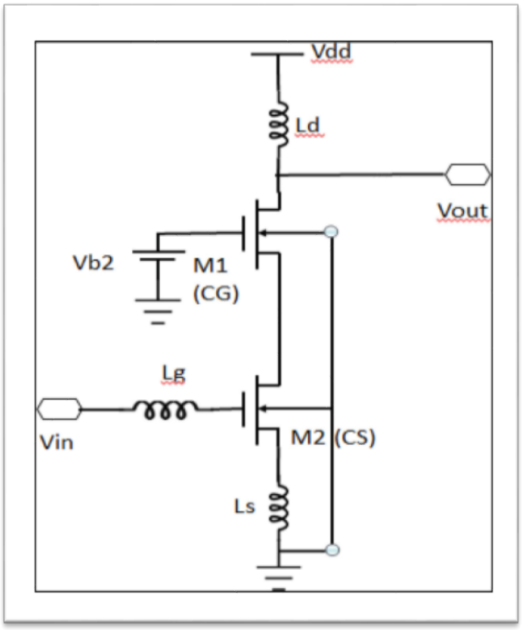

Fig. 3 Brokaw BGR

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A voltage reference circuit with an output voltage of about 1.25 V and little temperature sensitivity is known as a brokaw bandgap reference. One sort of voltage ref, this particular circuit is called for the first creator of the design, Paul Brokaw. The circuit maintains two internal voltage sources, one of which has a positive temperature coefficient and the other of which has a negative coeff, just like all temperature-independent bandgap references. The temperature dependence can be eliminated by adding the two together. A temperature sensor can also be made from one of the two internal sources. One of the base-emitter voltages and a number of base-emitter voltage discrepancies are added to produce the circuit output. The two opposing temperature coefficients will precisely cancel each other out with the right component selections, resulting in an output that is temperature independent

IV. RESULTS AND DISCUSSION

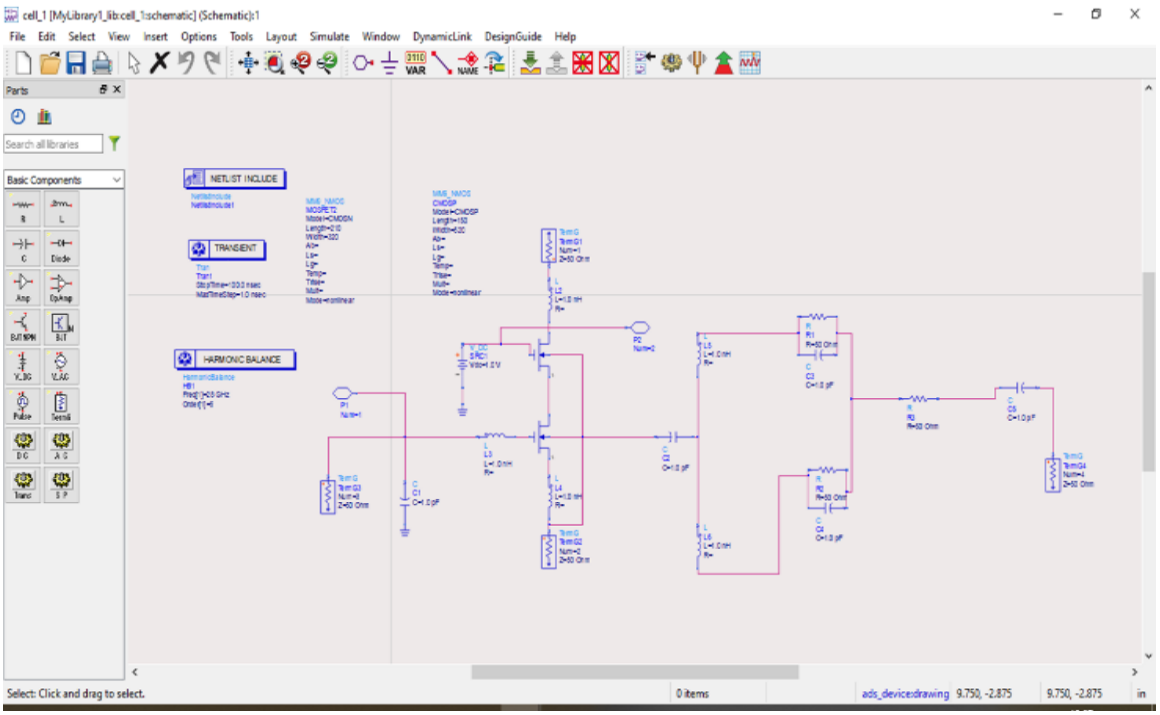

Fig. 4 Traditional brokaw BGR

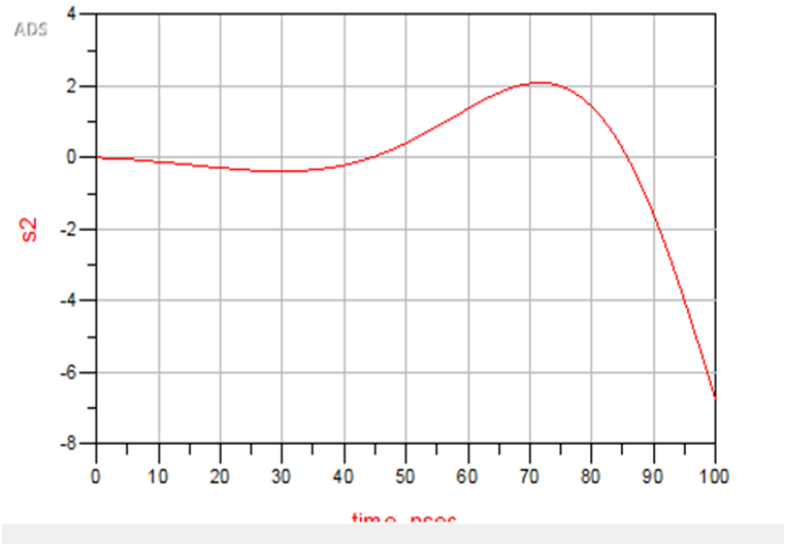

Fig. 5 Voltage reference Vref

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The voltage reference obtained from the above graph is 2.3 V

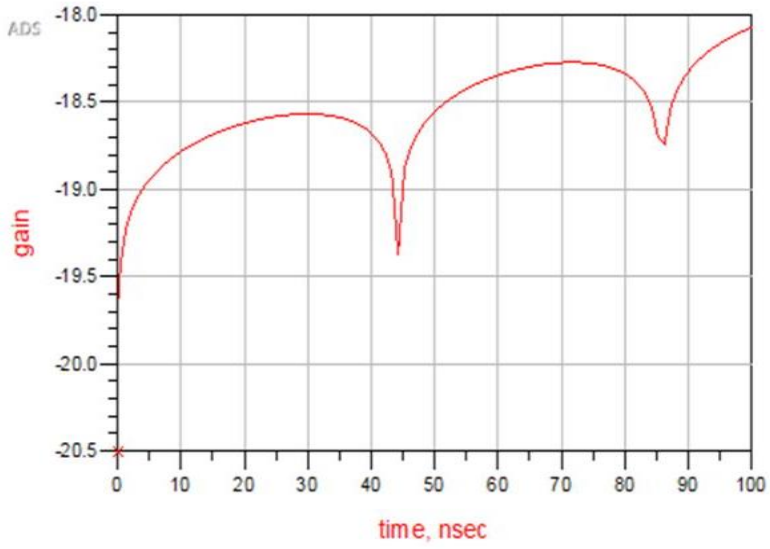

Fig. 6 PSRR

The power supply rejection ratio (PSRR) standard, which is frequently used with operational amplifiers and linear circuits, should be understood by analog designers. In these situations, PSRR is essentially an AC specification that gauges how much a circuit's output is attenuated by signals superimposed on power supplies as a function of frequency. Although PSRR is frequently included on data sheet specifications, it is typically not assessed in the same way, even though it may be just as significant for the A/D converter in a signal processing system.

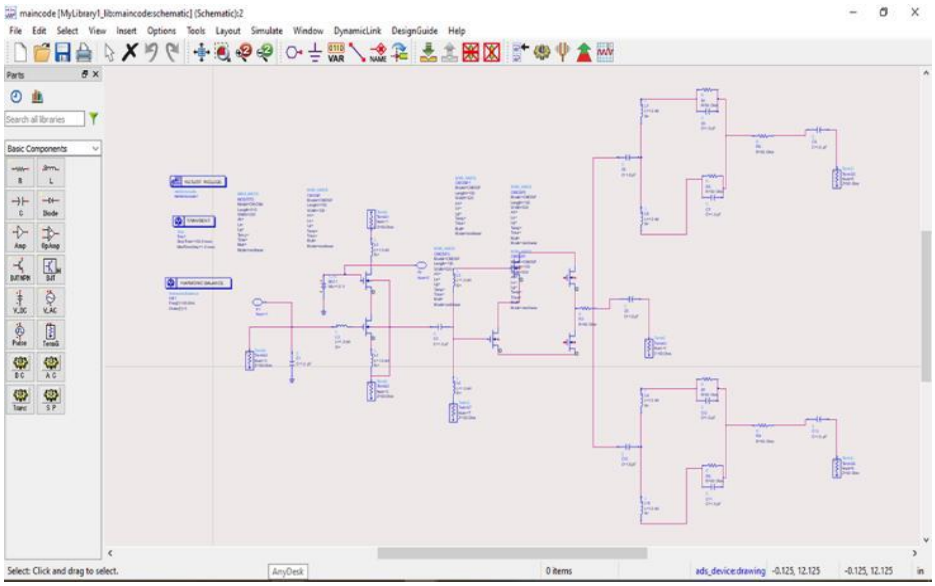

Fig. 7 Key figure BGR

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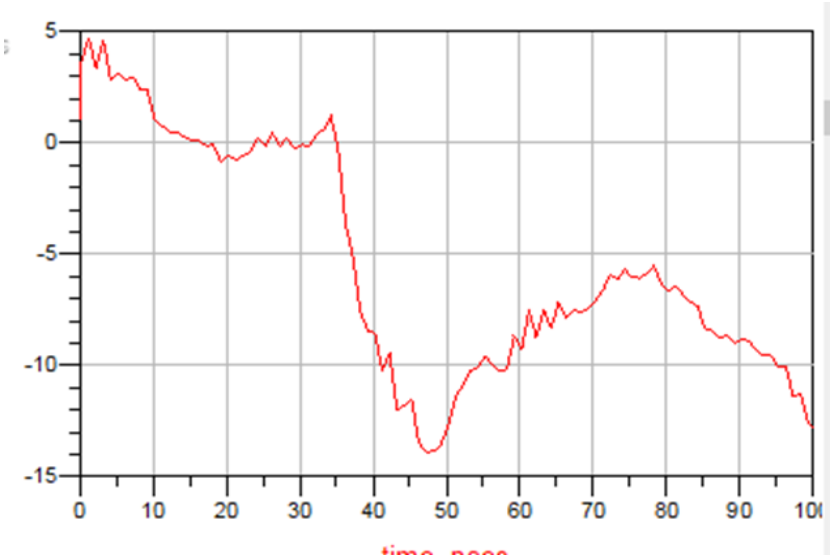

Fig. 8 Settling time graph

The time that has passed between the application of an ideal instantaneous step input and the time at which the amplifier output has entered and remained within a given error band is known as the settling time of a dynamical system in control theory, such as an amplifier or other output device. The time needed for the output to slew to a location near the final value, recover from the overload condition associated with the slew, and then settle to within the specified error is included in the settling time, along with a propagation delay. When exposed to inputs or disturbances, systems with energy storage cannot react instantly and will instead show temporary reactions

V. CONCLUSION

On the basis of the conventional Brokaw BGR, a CMOS BGR is created. According to the simulation findings, at the working voltage of 1.8V, the Vref is 2.3 V from 0 to 100s over the temperature range of -40 to 125, and the reference voltage fluctuates within 0.142mV when the power supply changes from 1V to 2.5V. The good power supply rejection is implied by the PSRR, which is 180.5dB. The power usage is merely 0.412mW. The suggested BGR has a wide range of applications for low-voltage analog integrated circuits. The BGR can be used in Low Voltage analog integrated circuits.

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