IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

3rd-International Conference on Muti-Disciplinary Application & Research Technologies (ICMART-2024)

Geetanjali Institute of Technical Studies

Vol. 11, Special Issue 2, May 2024

# Revolutionizing Electronics Packaging Exploring the Latest Developments in Thermal Meta-materials and Their Future Applications

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**Abstract:** Thermal metamaterials offer unique capabilities in controlling heat transfer, surpassing natural thermal properties through deliberate design. Recent advancements have enabled the manipulation of conductive heat transfer, leading to innovative structures like thermal cloaks and concentrators. These developments open new avenues for guiding heat in complex systems and revolutionizing electronics packaging's thermal management.

As electronics packaging trends toward higher power, density, and 2.5D/3D integration, effective thermal management becomes increasingly crucial. Traditional cooling methods using large thermal-conductivity materials, heat pipes, and heat exchangers may distribute heat uniformly but struggle with thermal crosstalk and local hot spots. Thermal metamaterials offer a deterministic approach to dissipate heat, potentially mitigating these challenges.

This paper reviews recent breakthroughs in thermal metamaterials relevant to electronics packaging. It delves into state-of-the-art techniques and critical challenges in 2.5D/3D-integrated packaging, highlighting how thermal metamaterials could reshape electronic packaging's thermal management landscape. Addressing these challenges requires further research into implementing thermal metamaterial designs in high-performance heterogeneous packages, pushing the boundaries of electronics packaging's capabilities.

**Index Terms:** Thermal metamaterial, Heat transfer control, Electronics packaging etc

## I. INTRODUCTION

Metamaterials are engineered structures designed to possess unique properties not found in natural materials. Recent advancements in optical metamaterials have revolutionized the control of light and electromagnetic waves. One remarkable achievement, the invisibility cloak, has been realized in microwave [1,2] and optical [3–8] frequencies using transformation optics principles. This connection between metamaterial properties and thermal dissipation has spurred interest in thermal metamaterials for heat management. Conduction-based thermal metamaterial have been demonstrated through numerical simulations [9–11] and experimental validations [12–15] under various conditions. Additionally, scattering cancelation-based bilayer thermal cloaks have been experimentally shown in 2D [16,17] and 3D [17,18] configurations. Techniques like topology optimization-based finite element methods [19,20] enable precise heat flow control in complex geometries, including noncircular or non-spherical shapes, and facilitate bi-functional cloaking [21]. Researchers have also explored manipulating both thermal and dc fields [22], as well as optimizing thermal-composite designs for managing heat in printed circuit board (PCB)-based electronics [23]. While thermal radiation-based metamaterials [24] are actively researched, they are not extensively covered here due to their limited relevance to electronic packaging.

Certainly, thermal metamaterials hold great promise for enhancing electronic packaging [25]. As nano-electronics, 3D-integrated circuits (ICs), and flexible electronics advance rapidly, managing heat becomes increasingly challenging [26]. For instance, in 2.5D packages, both logic power and the number of high-bandwidth memory (HBM) layers are on the rise [27,28]. A significant challenge in these packages is thermal crosstalk, where the logic chip and HBM, operating at different temperatures, are placed in close proximity [29,30]. This scenario calls for thermal metamaterials to aid in heat dissipation and safeguard temperature-sensitive components [31–33]. In 3D packages, thermal resistances and operating temperatures are also escalating. Traditional thermal management strategies involve optimizing through-silicon-via configurations [34–40] and employing single- or two-phase cooling systems with micro channels [41–46].

In this article, we provide a review and summary of recent advancements and future prospects in thermal metamaterials for addressing thermal management challenges in electronic packaging. Section 2 focuses on reviewing thermal metamaterials, emphasizing anisotropic heat spreaders and diffusers, thermal cloaking and isolation techniques, and devices for heat guiding and bending. This section covers both theoretical developments and experimental progress in thermal metamaterials relevant to packaging applications. In Section 3, we delve into the thermal management challenges associated with heterogeneous integration, particularly focusing on multichip implementations and multilayer stacking. Section 4 discusses the cooling capabilities at the package level and explores the potential impact of thermal metamaterials on packaging applications, along with potential avenues for future research.

## II. ADVANCEMENTS IN THERMAL METAMATERIALS

Over the past decade, there has been notable progress in the realm of thermal metamaterials. This progress has seen a shift towards practical applications, including thermostats [47], thermal camouflage [48], dual-function thermal metamaterials [49], and active heat flow control [50,51]. This section focuses on reviewing recent advancements in conduction-based thermal metamaterials specifically applicable to potential electronic packaging applications.

a) Anisotropic Heat Spreader: Controlling thermal energy transmission holds immense importance beyond basic research. Heat transfer is challenging to control within a single material or device due to the complex spectrum of high-frequency phonons. Microscale heat transport in solids follows Fourier's law of heat conduction: $q_i = -k_{ij} \blacktriangledown T_j$

Where heat flux ($q_i$) is proportional to the temperature gradient ($\blacktriangledown T_j$) via the thermal-conductivity tensor ($k_{ij}$ ) Engineering materials with specific anisotropy in their thermal conductivity can manipulate heat conduction paths effectively. For functional thermal devices, Chang et al. pioneered the development of thermal diodes using carbon and boron nitride nanotubes, exploiting non-uniform mass distribution for enhanced conductance. Similarly, 2D materials like black phosphorus exhibit thermal conductivity anisotropy due to their unique phonon dispersion properties.

b) Heat Cloaking and Isolating

Thermally sensitive elements or electronic systems benefit from being placed in regions with minimal thermal disturbances, termed thermal cloaks. These cloaks create near-zero thermal gradients across elements, regardless of surrounding temperature changes. Thermal cloaking involves bending heat flux through metamaterial arrangements, leading to applications like thermal concentrators or cloaks where temperature gradients can be engineered to zero. Experimental measurements have shown minimal temperature gradients (less than 0.004 K/cm) in cloaked regions, reducing temperature disturbances and offering potential for various thermal management functions. Research in thermal cloaking often focuses on hiding objects from external heat flow, employing coordinate transformation methodologies to achieve invisibility. Bi-functional cloaks with electrical and thermal cloaking functionalities have been developed, utilizing anisotropic thermal conductivity through nanoparticle-filled substrates and realistic diffusivity in multilayered cloaks.

c) Heat Guiding and Bending

As electronics become densely packed, efficient heat dissipation is crucial to minimize thermal crosstalk and protect sensitive components. While complex thermal metamaterials can manipulate heat flow, they are often costly to fabricate due to their intricate structures. In contrast, thermal shifters made of two isotropic materials offer manufacturability and the ability to bend heat flux as needed. By stacking materials with different thermal conductivities, such as copper and stainless steel, the heat flux can be rotated by varying the composite layer orientation. A higher thermal-conductivity ratio between materials results in a greater heat flux rotation angle, providing a practical approach to heat management in densely packed electronic systems.

## III. THERMAL MANAGEMENT CHALLENGES

### 3.1 *Thermal Challenges Due to 2.5 D-Dimensional Implementation*

In 2.5D package configurations, chips are integrated within a single interposer regardless of their node processes. This setup aims for improved performance, tighter tolerance, and increased power efficiency, essential for compact heterogeneous packages. Placing high-power chips closer together minimizes package size while addressing thermal management challenges like high power density, thermal crosstalk, temperature variations, selection of thermal interface materials (TIMs), and managing substrate thermal resistance.

- *High Power Density*

The challenge in thermal management for 2.5D packages arises from escalating power densities, exceeding 100W/cm^2 in some cases. Silicon interposers connect high-power logic chips and HBMs, necessitating efficient cooling close to heat sources. However, layers like TIM and heat slugs, although crucial for reliability, can increase thermal resistance.

Rising logic power and stacked HBMs amplify performance demands, highlighting the need for efficient cooling solutions at both system and board levels. Thermal metamaterials offer potential for enhanced heat flux control, particularly in board-level cooling scenarios.

- *Thermal Crosstalk*

In advanced heterogeneous packages like 2.5D platforms, close proximity of logic devices and HBMs within 500 μm can lead to thermal crosstalk issues affecting neighboring units. This crosstalk can increase leakage power and worsen self-heating effects. To mitigate this, options include increasing distance between logic chips, using low-thermal-conductivity materials for thermal barriers, or employing thermal metamaterial designs for controlled heat dissipation to a heat sink.

- *Differences in Operating Temperature and Power Generation*

In heterogeneous packages like 2.5D platforms, each device has a maximum operation temperature that should not be exceeded (e.g., 125°C for logic chips and 85°C for memory chips). Thermal crosstalk between adjacent chips with different temperature limits can lead to exceeding these limits, especially when high-power logic chips cause significant thermal effects on memory chips.

- *Thermal Interface Material Issues*

Thermal interface materials (TIMs) play a critical role in thermal management, with their performance influenced by thermal conductivity and bond layer thickness (BLT). In 2.5D packages, TIMs are commonly used between ASICs and HBMs. Due to differences in thermo mechanical properties, using different TIMs or adjusting device heights based on TIM compression characteristics can optimize performance. Substrate size can impact TIM performance, affecting voiding and drying out with temperature changes. Power thermal cycle inspection helps select TIMs with minimal performance impact. Metamaterial design principles offer potential for fabricating multilayer TIMs with controlled thermal properties.

- *Thick Substrate*

In advanced heterogeneous packages, placing multiple devices on one substrate increases the effective substrate thickness, raising vertical thermal resistance. Thick substrates pose significant thermal challenges in 2.5D integration. Thermal metamaterials can improve heat transfer through the substrate when integrated with interposer design. Other thermal solutions like thermal vias, metal cores, and metal blocks are also options for addressing these challenges.

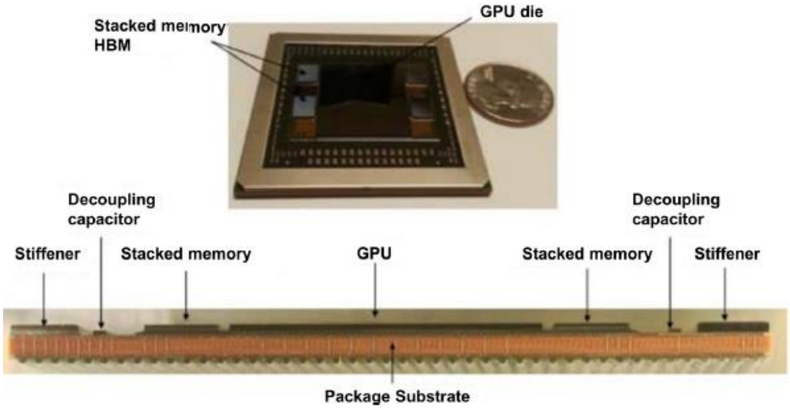

Fig. 1 Si Interposer with a 2.5D package. HBM size is 7.75mm311.87mm3720 lm. (Figure reprinted with permission from Lee et al. [108]. Copyright 2016 Institute of Electrical and Electronics Engineers.) [1]

*a. Thermal Challenges Due to Three-Dimensional Implementation*

In 3D package platforms, similar to 2.5D designs, heterogeneous integration aims for compactness and improved performance. However, stacking chips in 3D configurations introduces complex thermal challenges such as heat removal through stacked chips, thermal resistance in joint layers, limited thermal spreading with thinned chips, and solutions involving through-silicon vias (TSVs) for heat dissipation.

- *Heat Removal Through Stacked Chips*

In 3D chip stacks, the closest die to the substrate is typically the hottest due to I/O count or performance reasons. Heat from this hot chip dissipates through the stacked devices, posing thermal management challenges as each chip adds thermal resistance. Efficient cooling requires locating the hottest device near the cooling system or establishing a direct heat path to enhance cooling efficiency. Aditya et al. demonstrated thermal advantages in the TSV-SIP package platform.

- *Die Bonding*

In 3D stack platforms, chip bonding, especially the joint layer with micro bumps and a nonconductive film (NCF), significantly increases vertical thermal resistance.

- Thinning chips

Thinning chips can enhance heat spreading within the chip, particularly if package thickness is not limited.

## IV. THERMAL METAMATERIALS AND COOLING SOLUTIONS FOR PACKAGING

Increasing demands for advanced electronic devices have led to high-density packaging, driven by integrating more functions into individual chips. Scaling of devices and interconnects has also increased power density, with expectations of exceeding 1 kW/cm$^2$ for next-generation devices. These high heat fluxes present challenges like electro migration, material creep, thermal cycling, and warpage, emphasizing the importance of effective thermal design and architecture to maintain reliable electronics operation.

## V. CONCLUSION

This paper reviews recent progress in conduction-based thermal metamaterials and their potential applications in electronic packaging, addressing challenges like thermal crosstalk and local hot spots in 2.5D and 3D packages. Thermal metamaterial designs offer deterministic control over heat transfer paths, benefiting next-generation electronics and photonics. The review covers anisotropic heat spreaders, cloaking/isolating methods, and heat guiding/bending approaches, analyzing thermal challenges in advanced heterogeneous packaging for both lateral and vertical chip arrangements.

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