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Hardware Accelerator for Sign Language Detection on FPGA

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Abstract: This project aims to develop a hardware accelerator for real-time sign language detection using Atlera DE10-Lite FPGA board. Sign language recognition is essential for bridging communication gaps between sign language users and the broader population. By leveraging the parallel processing capabilities and energy efficiency of FPGAs, the system ensures low latency and high accuracy in gesture recognition.

The approach involves designing an optimized Convolutional Neural Network (CNN) architecture tailored for FPGA implementation and incorporating preprocessing techniques to enhance robustness against environmental variability.

Keywords: Hardware Accelerator, Convolutional Neural Network, Sign language detection, Altera DE10-Lite FPGA.

I. INTRODUCTION

This project focuses on the development of a hardware accelerator using FPGA (Field-Programmable Gate Array) to enable real-time, high-accuracy sign language detection. A hardware accelerator is a specialized computing component designed to perform specific tasks more efficiently than general-purpose processors by offloading computationally intensive operations. These accelerators can significantly improve performance in applications such as deep learning and signal processing by reducing latency and enhancing throughput.

FPGAs are particularly well-suited for hardware acceleration due to their ability to support parallel processing, flexibility, and customization. Unlike traditional CPUs or GPUs, FPGAs can be reconfigured to perform specific tasks optimally, which makes them highly efficient for real-time applications. In the context of sign language detection, this means FPGAs can execute gesture recognition algorithms with much faster processing speeds and lower energy consumption, making them ideal for embedded systems.

Sign language detection is an essential technology for bridging communication gaps between sign language users and those who do not understand it. By translating hand gestures into spoken or written language, this system enables better communication for the deaf and hard-of-hearing community.

The proposed FPGA-based hardware accelerator will combine the strengths of deep learning and FPGA technology to optimize the performance of sign language detection systems. It aims to minimize latency and maximize recognition accuracy, making the system suitable for real-world applications in fields such as healthcare, education, and human-computer interaction. By integrating CNNs with FPGA accelerators, the system can achieve seamless, real-time sign language recognition, thus improving communication accessibility.

II. LITERATURE SURVEY

[1] Varadala Sridhar. "Convolutional Neural Networks Based Sign Language Interpreter" (2024)
This paper presents an innovative CNN-based system to interpret sign language gestures in real time, addressing the communication gap between sign language users and others. The proposed framework involves preprocessing video data to isolate hand gestures and eliminate noise, ensuring high-quality input for the CNN model. The author emphasizes the importance of lightweight architectures to achieve low latency and make the system viable for real-time applications on constrained hardware. The system is evaluated on publicly available datasets and achieves state-of-the-art accuracy with minimal processing delays, demonstrating its practical utility in real-world scenarios.

The study further delves into optimizing the CNN architecture to reduce the computational load without compromising accuracy. Techniques such as dropout, batch normalization, and activation function tuning are employed to enhance performance.

Additionally, the author discusses the potential for integrating this system into portable devices like smartphones or kiosks. This work is highly relevant to your project as it offers a comprehensive methodology for real-time gesture recognition, which can be adapted for FPGA implementation to meet similar low-latency and accuracy demands.

[2] Sarkhel H. Taher Karim, Muhammed Latif Mahmood, Siva Sabir Abdulla, Shano Ali Abdulla. “Kurdish Sign Language Recognition Using CNN” (2024)
This paper addresses the underrepresentation of Kurdish sign language in computational linguistics and proposes a CNN-based model tailored for recognizing gestures specific to this language. The authors create a novel dataset of Kurdish sign gestures, tackling challenges such as gesture variations across individuals and the lack of standardized training data. The system preprocesses images to enhance feature visibility and applies CNNs to classify gestures, achieving satisfactory results even with limited data. Comparisons with traditional machine learning models reveal the superior performance of CNNs in handling complex gesture patterns. The researchers highlight the importance of dataset quality and size in training robust deep learning models. They also explore strategies to generalize the model to unseen data by employing data augmentation and regularization techniques. For your project, this study demonstrates how to adapt CNNs to underrepresented languages and datasets, offering insights into managing data scarcity, which could be critical if you plan to develop your own gesture dataset.

[3] Haobo Ye. “Accelerating Convolutional Neural Networks: Exploring FPGA-Based Architectures and Challenges” (2024)
This paper investigates FPGA-based acceleration for CNNs, focusing on design considerations and trade-offs for achieving optimal performance. The author explores key architectural techniques such as pipelining, parallel processing, and tiling to optimize computational throughput while managing resource constraints. By mapping CNN layers to FPGA resources efficiently, the study demonstrates significant improvements in latency and energy efficiency compared to GPU implementations. Challenges such as memory bandwidth limitations and kernel size optimization are discussed, with practical solutions proposed for each. Additionally, the paper highlights emerging trends in FPGA-based deep learning, such as the use of High-Level Synthesis (HLS) tools to streamline development. Performance benchmarks provided for standard CNN architectures like ResNet and VGGNet reveal the feasibility of deploying complex models on FPGA without sacrificing accuracy. This work is directly relevant to your project, offering technical insights into overcoming hardware constraints while accelerating CNN inference for real-time applications like sign language recognition.

[4] Muthukumaran Vaithianathan et al. “Comparative Study of FPGA and GPU for High-Performance Computing and AI” (2023)
This paper compares the computational efficiency of FPGA and GPU platforms in high-performance computing (HPC) and AI applications. It provides a detailed analysis of their architectures, focusing on how GPUs excel in parallel processing for high-throughput tasks, while FPGAs offer deterministic latency and superior energy efficiency. The authors emphasize that FPGAs are particularly advantageous for applications requiring real-time inference, as their reconfigurable nature allows for task-specific optimizations. Benchmarks of AI workloads, including CNNs, highlight scenarios where FPGAs outperform GPUs, especially in power-constrained environments. The paper also explores hybrid approaches, where FPGAs and GPUs are used in tandem to balance performance and efficiency. This study is highly relevant for your project, as it provides a strong case for choosing FPGA for implementing low-latency, energy-efficient systems. The insights from the benchmarks and architectural comparisons can guide your design decisions, ensuring optimal utilization of FPGA resources for gesture recognition tasks.

[5] Haochen Shi. “FPGA Hardware Acceleration Design for Deep Learning” (2023)
This paper focuses on designing FPGA-based hardware accelerators for deep learning tasks, particularly CNNs. It introduces innovative techniques to optimize resource allocation, including layer-wise resource partitioning and quantization, to accommodate large models within FPGA’s resource constraints. High-Level Synthesis (HLS) tools are utilized to simplify the design process, enabling faster prototyping and iteration. The proposed accelerators are evaluated on popular deep learning models, demonstrating significant improvements in inference speed and energy consumption compared to CPU and GPU implementations. The author also discusses the importance of balancing computational throughput with memory bandwidth, a critical factor in FPGA-based designs. Strategies like data reuse and on-chip caching are explored to enhance efficiency further. This work is particularly relevant to your project as it provides actionable strategies for designing FPGA accelerators for CNNs, ensuring high performance and energy efficiency in real-time applications like sign language detection.

[6] Zhi Qi et al. “Designing Deep Learning Hardware Accelerator and Efficiency Evaluation” (2022)
This paper focuses on the design and evaluation of efficient hardware accelerators for deep learning applications, particularly on FPGA platforms. The authors propose architectural enhancements such as pipelining, loop unrolling, and

task-level parallelism to optimize throughput and latency. Detailed case studies are provided, comparing various FPGA configurations for implementing deep learning models like AlexNet and ResNet. The work also emphasizes resource-aware design, balancing logic usage, memory bandwidth, and power consumption to achieve maximum performance. Efficiency evaluation frameworks introduced in this paper incorporate metrics such as latency, power efficiency, and accuracy retention, providing a holistic approach to assessing hardware accelerators. The study concludes that FPGA accelerators, with their reconfigurability and energy efficiency, are highly suited for edge AI applications. For your project, this paper serves as a guide for implementing and evaluating FPGA-based designs for CNNs, ensuring that the hardware achieves the desired performance while remaining resource-efficient.

[7] Vijeeta Patil et al. "A Deep Learning Framework for Real-Time Sign Language Recognition Based on Transfer Learning" (2022)
This work leverages transfer learning to develop a deep learning framework for real-time sign language recognition. By using pre-trained models such as MobileNet and ResNet, the authors reduce the training time and computational complexity typically associated with CNNs. The framework incorporates preprocessing techniques like background subtraction and motion detection to focus on hand gestures and minimize noise in input video streams. Experimental results show that the system achieves high accuracy on benchmark datasets, demonstrating its potential for real-time applications. The study also explores techniques to enhance generalization, such as fine-tuning pre-trained layers and employing data augmentation. These strategies make the framework robust to variations in signer demographics and environmental conditions. The use of lightweight pre-trained models is particularly relevant for your project, as it aligns with the constraints of deploying CNNs on FPGA platforms. This paper provides valuable insights into integrating transfer learning for sign language recognition, improving both accuracy and computational efficiency.

[8] Ran Wu et al. "Accelerating Neural Network Inference on FPGA-Based Platforms—A Survey" (2021)
This comprehensive survey reviews FPGA-based methods for accelerating neural network inference, covering a range of applications from computer vision to natural language processing. The authors detail optimization techniques such as quantization, pruning, and hardware-aware neural architecture search (NAS), highlighting their impact on performance and resource utilization. Challenges like limited on-chip memory and high design complexity are addressed, with proposed solutions to mitigate these issues. The paper also examines trends in FPGA-based acceleration, including the adoption of high-level synthesis (HLS) tools and integration with cloud-based platforms. Detailed benchmarks illustrate the advantages of FPGA accelerators over traditional hardware, especially in latency-sensitive applications. For your project, this survey serves as an invaluable resource for understanding the landscape of FPGA-based deep learning accelerators, offering a roadmap for tackling the challenges involved in deploying CNNs on reconfigurable hardware.

[9] Razieh Rastgoo et al. "Sign Language Recognition: A Deep Survey" (2021)
This survey provides a comprehensive overview of sign language recognition (SLR) techniques, with a particular focus on deep learning-based approaches. The authors categorize existing systems based on input modalities (e.g., images, videos, or sensor data) and explore their respective strengths and limitations. Recent advancements in SLR are highlighted, including the use of advanced CNN architectures, attention mechanisms, and multimodal learning. Key challenges such as signer variability, gesture ambiguity, and the scarcity of large, annotated datasets are discussed in detail. The paper emphasizes the importance of preprocessing and feature extraction in achieving robust SLR systems. It also explores the potential of real-time applications, identifying hardware constraints and computational requirements as key barriers. For your project, this paper provides a solid theoretical foundation, highlighting the state-of-the-art techniques and gaps in SLR research that your FPGA-based system could address, particularly in real-time scenarios.

[10] Duy Thanh Nguyen et al. "A High-Throughput and Power-Efficient FPGA Implementation of YOLO CNN for Object Detection" (2019)
This paper focuses on implementing the YOLO (You Only Look Once) CNN for object detection on FPGA platforms. The authors develop a high-throughput, power-efficient design by optimizing layer computations, leveraging parallelism, and reducing memory accesses. Techniques such as quantization and pipelining are employed to adapt the YOLO model to FPGA's hardware constraints without sacrificing detection accuracy. Experimental results show that the FPGA implementation achieves real-time performance with significantly lower power consumption compared to GPU-based solutions. The study also highlights design challenges, such as balancing computation and memory bandwidth, and provides strategies to overcome them. The insights from this work are particularly valuable for adapting complex CNN models to FPGA hardware. While the focus is on object detection, the techniques used for optimization and power efficiency are directly applicable to your project, especially in designing low-latency FPGA-based accelerators for sign language recognition.

[11] Dai Rongshi and Tang Yongming. "Accelerator Implementation of LeNet-5 CNN Based on FPGA with HLS" (2019)
This paper explores the implementation of the classic LeNet-5 CNN architecture on FPGA using High-Level Synthesis (HLS) tools. The authors detail the process of converting the LeNet-5 model into an efficient hardware design, focusing on the trade-offs between accuracy and resource utilization. Techniques such as loop unrolling, tiling, and pipelining are employed to optimize the performance of convolutional layers, ensuring low latency and high throughput. The FPGA implementation is benchmarked against CPU and GPU systems, demonstrating superior energy efficiency and comparable accuracy in image classification tasks. The study also highlights the flexibility offered by HLS tools in mapping deep learning models to FPGA hardware. Challenges such as managing on-chip memory and balancing computation workloads are addressed, providing insights into the design process. For your project, this paper offers practical guidance on using HLS tools to accelerate CNN models, which can be adapted for implementing sign language recognition systems. The focus on optimizing classic architectures provides a strong foundation for designing efficient hardware accelerators.

[12] Teng Wang et al. "An Overview of FPGA-Based Deep Learning Accelerators: Challenges and Opportunities" (2019)
This paper provides an in-depth overview of FPGA-based accelerators for deep learning, focusing on the unique challenges and opportunities associated with these platforms. The authors discuss the limitations of traditional hardware like CPUs and GPUs in handling energy-efficient real-time applications and highlight FPGAs as a viable alternative. Strategies such as dataflow architecture, weight quantization, and hardware-aware model pruning are explored to optimize deep learning performance on FPGA. The paper emphasizes the versatility of FPGA accelerators in supporting various deep learning tasks, from image recognition to natural language processing. It also identifies key bottlenecks, such as limited memory bandwidth and the complexity of programming FPGAs, and proposes solutions to address these issues. For your project, this paper serves as a valuable resource for understanding the broader context of FPGA-based deep learning acceleration, offering insights into overcoming hardware limitations to achieve high efficiency and low latency.

[13] Ahmad Shawahna et al. "FPGA-Based Accelerators of Deep Learning Networks for Learning and Classification: A Review" (2018)
This review paper examines FPGA-based accelerators for deep learning networks, focusing on their application in learning and classification tasks. The authors categorize existing accelerators based on their design methodologies, such as custom RTL design and HLS-based approaches, highlighting their respective advantages and trade-offs. Techniques like layer fusion, tiling, and pipelining are discussed in detail, showcasing how they improve computational throughput and resource utilization. The paper also evaluates the performance of FPGA accelerators in terms of latency, energy efficiency, and scalability, comparing them to traditional hardware platforms. Challenges such as handling large-scale networks and integrating accelerators into larger systems are addressed, with proposed solutions for each. This review is particularly relevant to your project, offering a comprehensive understanding of the current landscape of FPGA-based deep learning accelerators and guiding the design of your sign language recognition system.

[14] Tongtong Zhang et al. "FPGA-Based Implementation of Hand Gesture Recognition Using CNN" (2018)
This paper investigates the implementation of a hand gesture recognition system using CNNs on FPGA. The authors focus on optimizing the CNN model to fit within FPGA's resource constraints, employing techniques like quantization and weight pruning. The system preprocesses input images to extract hand regions and remove background noise, ensuring high-quality input for the CNN. Experimental results demonstrate real-time performance and high accuracy in recognizing gestures, making the system suitable for interactive applications. The study also explores the challenges of deploying CNNs on FPGA, such as balancing computation and memory usage. By leveraging FPGA's parallelism capabilities, the authors achieve significant reductions in inference latency compared to CPU-based systems. This work is directly applicable to your project, as it provides a practical example of implementing a gesture recognition system on FPGA, highlighting key design considerations and optimization strategies.

[15] Kaiyuan Guo et al. "A Survey of FPGA-Based Neural Network Accelerators" (2017)
This survey offers a comprehensive overview of FPGA-based neural network accelerators, focusing on their design methodologies, performance metrics, and application areas. The authors analyze various accelerator architectures, discussing how techniques like pipelining, quantization, and memory optimization improve efficiency. The survey also highlights emerging trends, such as hardware-aware neural architecture search (NAS) and the integration of accelerators into edge devices. The paper identifies key challenges in FPGA-based acceleration, including managing on-chip memory, optimizing dataflow, and balancing accuracy with resource utilization. Solutions such as sparse computation and approximate computing are explored, showcasing their potential to enhance performance. For your project, this survey provides a foundational understanding of FPGA-based acceleration, offering insights into designing efficient hardware for real-time applications like sign language recognition.

III. CONCLUSION

In conclusion, the development of a hardware accelerator for sign language detection using FPGA presents an innovative approach to overcoming the communication gap between sign language users and non-users. The use of FPGA as a hardware accelerator allows for parallel processing and significant energy efficiency, enabling faster execution of complex gesture recognition algorithms, such as CNNs, in real-time. This system has the potential to be deployed in various practical applications, ranging from healthcare to education, and offers a solution to bridge communication barriers for the deaf and hard-of-hearing communities.

The literature survey indicates several promising future directions for enhancing this technology. There is significant potential to improve the performance metrics such as accuracy, latency, and energy efficiency. The performance metrics of gesture recognition, including classification accuracy and latency, will be a primary focus for future work. By exploring new techniques in FPGA design and optimization, the goal is to reduce inference latency further while improving the accuracy of gesture classification. Ultimately, this work aims to contribute to the ongoing development of more inclusive, efficient hardware accelerator and accessible sign language recognition system.

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