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Design and Implementation of FIR Filters Using Verilog

A.V. Muthyalamma[1], Dr.G. Srinivasa Rao[2], T.A.S. N Devi[3], Sk Munaz[4], Y. Vasundhara[5]

Assistant Professor, Electronics and Communication Engineering, Bapatla Women's Engineering College, Bapatla, India[1]

Professor, Electronics and Communication Engineering, Bapatla Women's Engineering College, Bapatla, India[2]

UG Students, Electronics and Communication Engineering, Bapatla Women's Engineering College, Bapatla, India[3,4,5]

Abstract: Finite Impulse Response (FIR) filters play a crucial role in digital signal processing applications, demanding high-speed and power-efficient arithmetic operations. The design and implementation of a 7-tap Finite Impulse Response (FIR) filter using Verilog is a crucial task in digital signal processing (DSP) applications. In this project, a high-performance, area-efficient, and fast 7-tap FIR filter is designed utilizing Kogge-Stone Adder (KSA) for the addition operations within the filter structure. The Kogge-Stone Adder, known for its parallel prefix structure and logarithmic delay, significantly improves the speed of the filter compared to conventional ripple-carry adders. The development process is carried out using Xilinx ISE 14.7 software, installed within a VirtualBox environment for compatibility and ease of access. The project covers the complete flow from RTL design, functional simulation, synthesis, and timing analysis.

Keywords: Digital Signal Processing, Finite Impulse Response Filter, Kogge-Stone Adder, Verilog, Xilinx ISE 14.7.

I. INTRODUCTION

Finite Impulse Response (FIR) filters are a type of digital filter commonly used in signal processing tasks. They are named for the fact that their response to an input signal eventually comes to zero after a limited number of steps. FIR filters are popular due to their straightforward design and inherent stability, since they do not use feedback from output to input.

In a typical FIR filter, the output signal is formed by multiplying recent input samples by a set of fixed coefficients and then summing the results. These coefficients define how the filter behaves and what frequencies it allows or blocks. A major benefit of FIR filters is their ability to maintain a linear phase, which means that all frequency components of a signal are delayed equally this is crucial in applications like audio or image processing where signal distortion must be minimized. Because of their predictable behavior and ease of implementation on digital systems, FIR filters are widely used in real-world applications such as communication systems, sensor data processing, and multimedia devices.

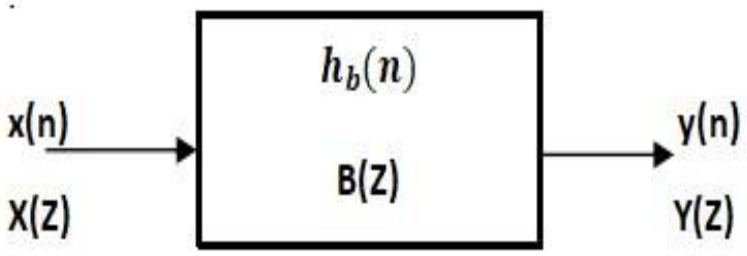

Fig 1. FIR Filter

In time domain: y(n)= x(n) * h_b(n)
In z-domain: Y(z)=B(z) X(z)

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A tap FIR filter is one type of digital filter used for the DSP application. The term “tap” refers to each delay-and-multiply stage in the filter's structure. The number of taps determines how many past input samples are used to compute each output sample, directly affecting the filter’s behaviour, accuracy, and complexity.

Tap FIR filter consists of the following components:

Delay elements: These store previous input samples.
Multipliers: Each delayed input is multiplied by a corresponding coefficient (weight).
Adders: The multiplied results are summed to produce the filter's output

II. LITERATURE REVIEW

[1] Suraj R. Gaikwad & Gopal S. Gawande (2014), this study uses MATLAB Simulink and Xilinx System Generator to design multi-stage FIR filters targeting audio signal decimation (from 128 kHz to 3.4 kHz). By dividing the filtering process into multiple stages, it significantly reduces filter order and improves computational and storage efficiency, making it suitable for FPGA implementation.

[2] Akshitha V Rameshetal. (2020) This work focuses on a 4-tap Moving Average FIR filter implemented using Verilog HDL and FPGA. It employs Multiply and Accumulate (MAC) operations and convolution techniques. The design is simple, stable, and ensures a linear phase response, suitable for basic DSP tasks.

[3] T. Thanmai& JVR Ravindra (2021) The authors propose a 5-stage FIR filter using a Modified Montgomery Multiplier to achieve high performance and low power consumption. The design leverages both MATLAB Simulink and Verilog HDL, targeting efficient architecture for real-time DSP systems.

[4] Dr. B. Rama Rao et al. (2022) This paper introduces a 6-tap FIR filter using a MAC structure that incorporates a Wallace Tree multiplier and binary adders to reduce power consumption. Coefficients are generated via MATLAB, and the filter is aimed at low-power embedded applications.

[5] Smitha N. Mallya's 2015 paper presents an efficient FIR filter multiplier design using techniques like Modified Booth Encoding and Carry Save Adders, implemented in Verilog on a Spartan 3E FPGA, achieving reduced power and faster performance.

[6] Ridhi Gupta et al. (2024) designed FIR filters using Verilog with windowing methods and Distributed Arithmetic, proposing a LUT-less approach to minimize memory usage and enhance

III. EXISTING METHOD

A 4-tap Finite Impulse Response (FIR) filter is a basic digital filter that processes discrete-time signals by convolving input samples with a set of four fixed coefficients. In this implementation, a Ripple Carry Adder (RCA) is used to perform the addition operations required in the convolution process. The FIR filter takes in four recent input samples, multiplies each with its corresponding coefficient, and sums the results to generate the output. The Ripple Carry Adder is a straightforward and easy-to-implement adder architecture where the carry-out of each bit addition is passed to the next bit in sequence.

An FIR (Finite Impulse Response) filter processes digital input samples to produce filtered output. A 4-tap FIR filter uses four coefficients (taps) and works according to the equation:

$y[n]=h0\cdot x[n]+h1\cdot x[n-1]+h2\cdot x[n-2]+h3\cdot x[n-3]$
therefore, h0, h1, h2, h3 are the filter coefficients (fixed constants).
$x[n]$, $x[n-1]$, $x[n-2]$, $x[n-3]$ are current and previous inputs.
y[n] is the output at time

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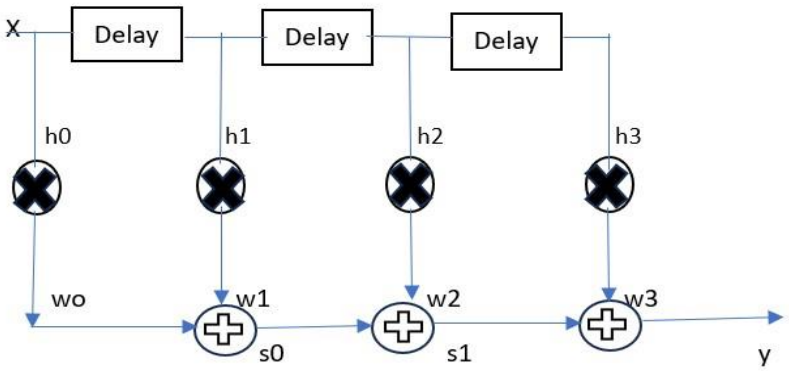

Fig 2.4 Tap FIR filter

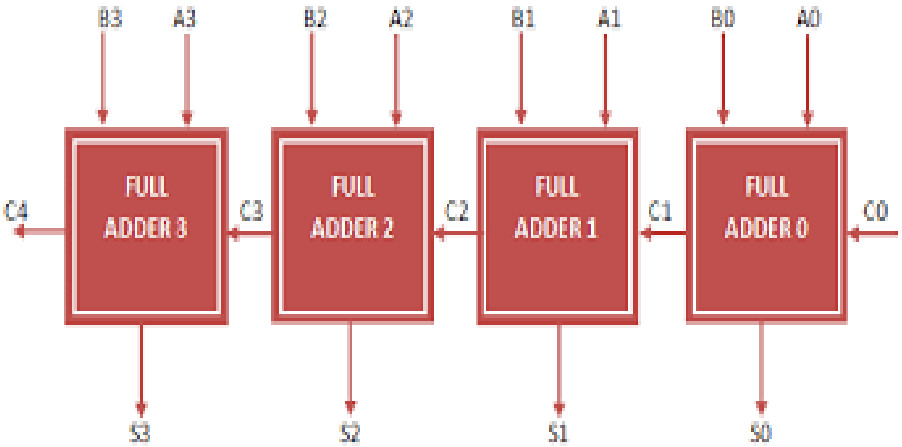

Fig3. Ripple Carry Adder

Results

RTL Schematic

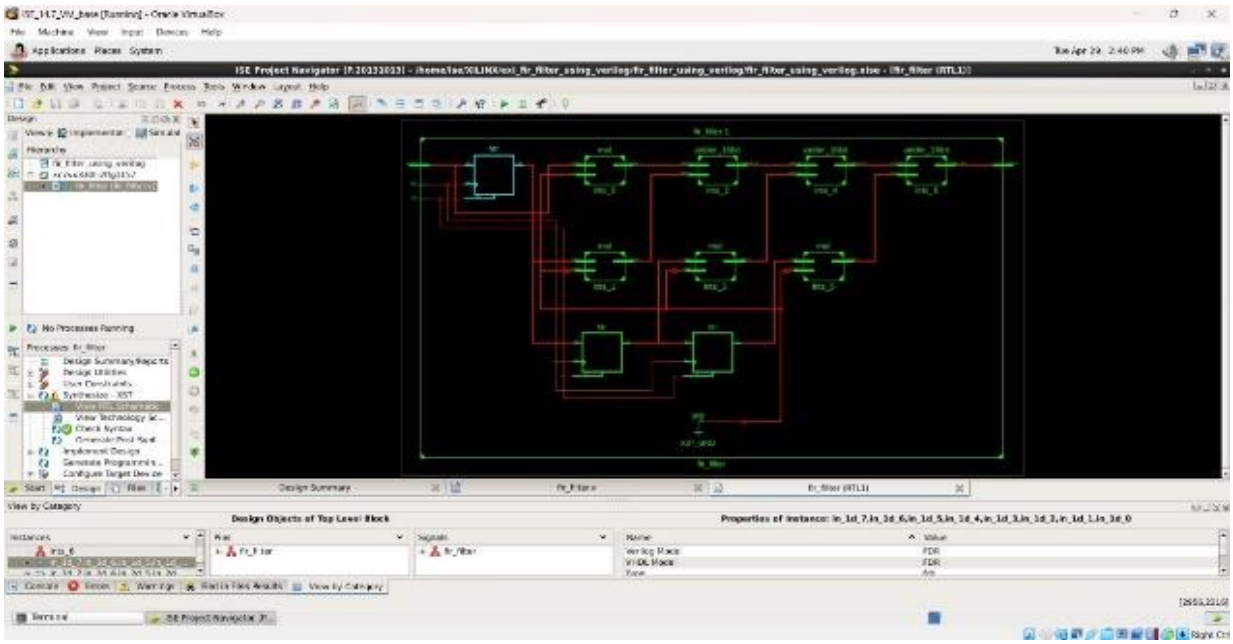

Fig4. RTL Schematic

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Timing Waveforms

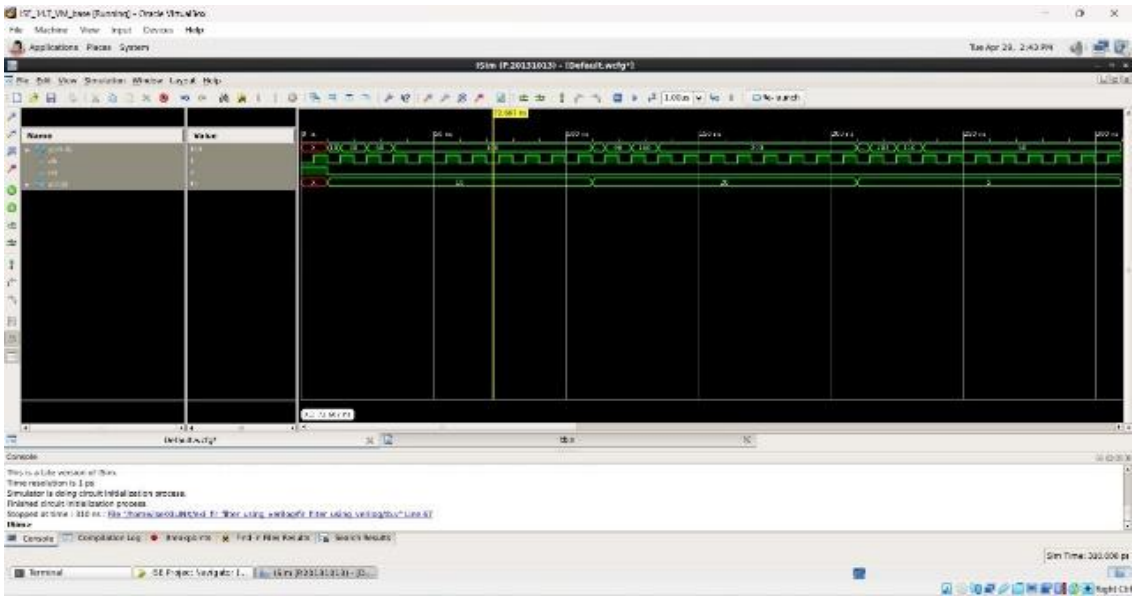

Fig5. Timing Waveforms

IV. PROPOSED METHOD

A 7-tap FIR (Finite Impulse Response) filter is a type of digital filter commonly used in signal processing applications to remove unwanted components from a signal or to enhance desired parts. The term 7-tap refers to the number of coefficients, used in the filter, which determines how many past input samples contribute to the current output. FIR filters are known for their stability and linear phase characteristics, making them ideal for applications where signal fidelity is important. The output of a 7-tap FIR filter is calculated as a weighted sum of the current input and the six most recent past inputs, with each input multiplied by a predefined coefficient. The Kogge-Stone Adder is a high-performance, parallel-prefix form of binary adder designed to achieve fast addition by minimizing carry propagation delay. This results in low logic depth and high-speed performance, especially beneficial in applications where rapid arithmetic computation is critical. Due to its parallelism and efficient carry generation, it is widely used in high-speed digital circuits such as arithmetic logic units (ALUs), signal processors, and custom hardware accelerators.

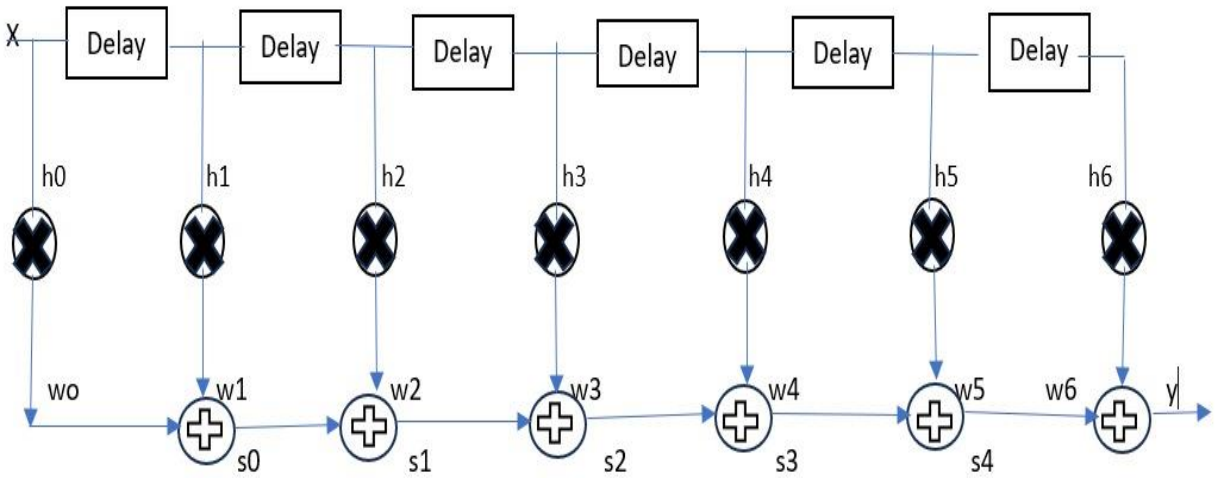

Fig 5. 7- Tap FIR Filter

In digital design projects like FIR filters, integrating a Kogge-Stone Adder enhances the throughput of the system by accelerating the addition of partial products, thereby improving the overall efficiency of the computation pipeline.

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In the 7-tap FIR filter design, the Kogge-Stone Adder is used in place of conventional adders to optimize the performance of the addition operations involved in convolution. Each output sample of a FIR filter requires multiple additions of products between input samples and filter coefficients. By replacing traditional adders like the Ripple Carry Adder with the Kogge-Stone Adder, the design achieves faster carry propagation and reduced computation delay, this significantly improves the overall speed and efficiency of the FIR filter, making it more suitable for high-performance and real-time digital signal processing applications.

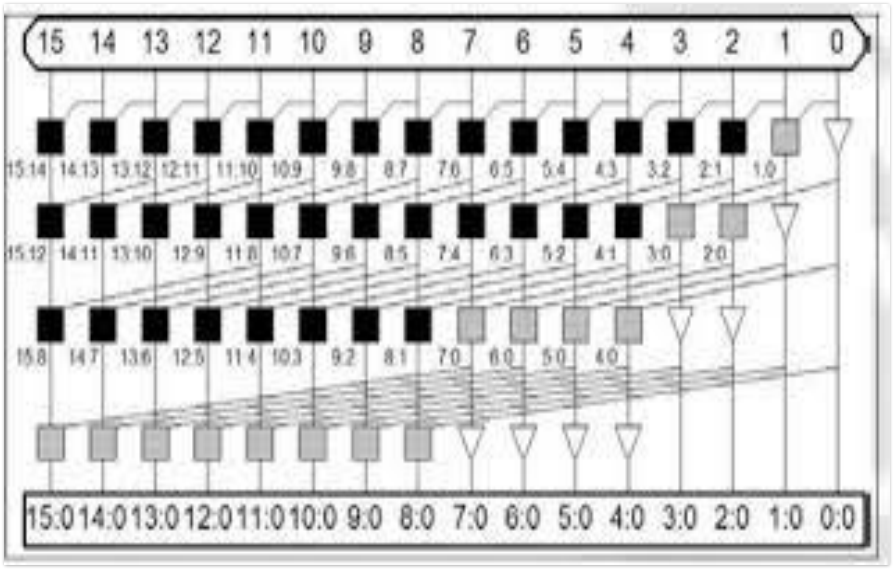

Fig 6. Kogge Stone Adder

Software Tool (Xilinx ISE 14.7)

Xilinx ISE 14.7 is an integrated software environment developed by Xilinx for digital circuit design and simulation using Hardware Description Languages (HDLs) such as Verilog. It provides a suite of tools for writing, compiling, simulating, synthesizing, and implementing digital designs. One of its strengths lies in its integration of synthesis, simulation, timing analysis, and bitstream generation within a single workflow, allowing for efficient progression from high-level code to hardware-ready output. For projects like a 7-tap Finite Impulse Response (FIR) filter, Xilinx ISE 14.7 proves to be an effective development platform. Implementing FIR filters in Verilog enables high-speed, customizable, and parallel signal processing.

Within ISE, users can describe the filter architecture, simulate functionality using ISim, and optimize the design through synthesis and timing analysis. ISim's waveform-based debugging helps identify logical errors and optimize signal flow in complex designs. Due to compatibility issues with modern operating systems, Xilinx ISE 14.7 is often run in a virtualized environment using tools like Oracle VirtualBox.

This setup involves configuring a virtual machine with adequate resources and installing a compatible OS along with the ISE software. Once installed, users create a new HDL project in ISE, write the Verilog code for the 7-tap FIR filter using a shift register and predefined coefficients, and set this module as the top-level design. A testbench is then created to simulate the filter, generate a clock and reset signal, apply input samples, and observe output responses.

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V. RESULT

RTL Schematic

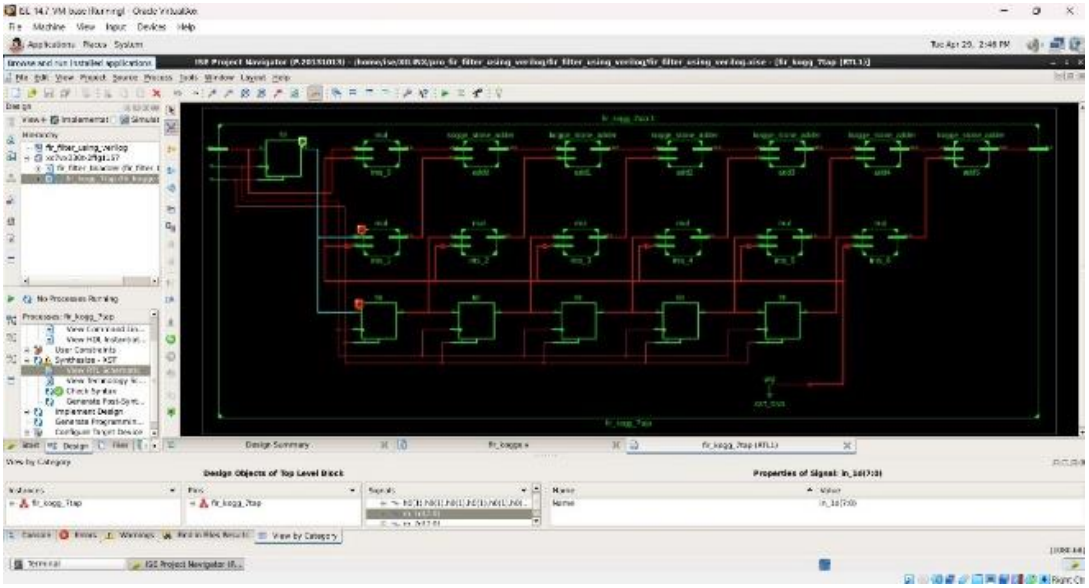

Fig 7. RTL Schematic

Timing Waveform

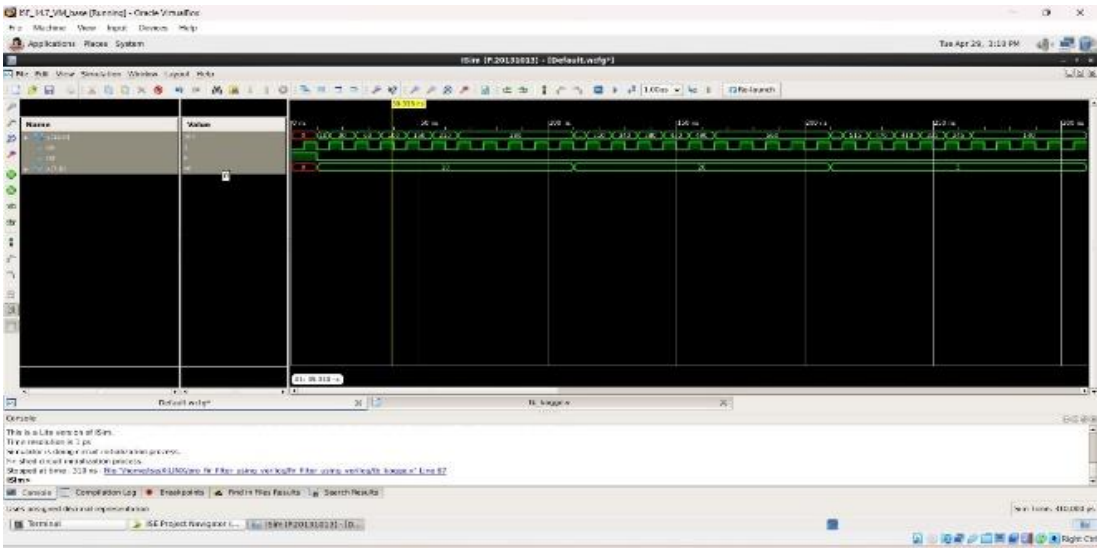

Fig 8. Timing Waveform

VI. CONCLUSION AND FUTURE SCOPE

In this project, a 7-tap Finite Impulse Response (FIR) filter was successfully designed, simulated, and implemented using Verilog Hardware Description Language (HDL). The design emphasizes high-speed digital computation, achieved through the optimization of arithmetic operations using a Kogge-Stone Adder a highly efficient parallel-prefix adder architecture. FIR filters are fundamental components in digital signal processing (DSP), often used in applications requiring linear-phase response and stability. The filter's performance heavily depends on its arithmetic units, particularly adders, which are frequently used in convolution operations.

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In this implementation, the Kogge-Stone Adder replaced traditional adders like the Ripple Carry Adder to minimize logic depth and maximize speed. Its parallel structure reduces carry propagation delay, thereby significantly enhancing the speed and efficiency of the FIR filter.

The 7-tap FIR filter design using the Kogge-Stone Adder offers a high-performance solution for digital signal processing, with demonstrated improvements in computational speed and efficiency. This design can be further enhanced by increasing the number of taps, which allows for more precise filtering, especially in applications requiring sharper cutoff frequencies or better attenuation in the stopband. A higher number of taps increases filter resolution, enabling the system to handle more complex signals with greater accuracy. Future work can explore multi-objective optimization strategies to balance speed, area, and power consumption, which are critical parameters in real-time embedded DSP systems. Techniques such as pipelining, parallel processing, and low-power design methodologies can be applied to adapt the filter for energy-constrained environments like mobile or wearable devices.

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