IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Impact Factor 8.066 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 12, Issue 5, May 2025

DOI: 10.17148/IARJSET.2025.12502

A 32-Bit MAC Unit Design Using Hybrid Multiplier with Reversible logic gates and Han-Carlson Adder

Kolati Srilatha[1], Dr. G. Srinivas Rao[2], P. Gayatri[3], P. Ramya[4], P. Nandini[5]

Assistant Professor, Electronics and Communication Engineering, Bapatla Women's Engineering College, Bapatla, India[1]

Professor, Electronics and Communication Engineering, Bapatla Women's Engineering College, Bapatla, India[2]

UG Student, Electronics and Communication Engineering, Bapatla Women's Engineering College, Bapatla, India[3,4,5]

Abstract: The Multiply-Accumulate (MAC) unit plays a pivotal role in digital signal processing (DSP), image processing, and embedded applications, where speed and power efficiency are of utmost importance. This paper proposes a novel 32-bit MAC architecture employing a hybrid Vedic multiplier and reversible logic gates, integrated with a Han-Carlson adder to enhance computational performance. The hybrid multiplier combines the advantages of traditional and Vedic techniques for faster partial product generation, while the use of reversible logic gates significantly reduces power dissipation, making the design suitable for low-power applications. The Han-Karlson adder, with its high-speed carry propagation and balanced logic structure, further accelerates the addition process. The proposed design is modelled and simulated using industry-standard tools and is evaluated against conventional MAC architectures in terms of delay, area, and power. Experimental results confirm that the proposed MAC unit achieves superior performance, offering a viable solution for next-generation VLSI systems.

Index terms: Multiply-Accumulate Unit (MAC), Vedic Multiplier, Reversible Logic Gates, Han-Karlson Adder, Low Power, High Speed, VLSI Design, Digital Signal Processing.

I. INTRODUCTION

The increasing demand for high-performance and low-power digital processing units has driven significant advancements in VLSI architecture, especially in domains such as digital signal processing (DSP), artificial intelligence (AI), and embedded systems. At the core of many such applications lies the Multiply-Accumulate (MAC) unit, fundamental arithmetic component responsible for performing critical operations in filters, transforms, and convolution engines.

Traditional MAC unit designs, though functionally effective, often suffer from limitations in terms of speed, area, and power consumption, particularly when scaled for higher bit-widths in modern systems. To address these challenges, this paper proposes a novel 32-bit MAC unit architecture that combines the strengths of three advanced design techniques: a hybrid Vedic multiplier, reversible logic gates, and the Han-Karlson adder. The hybrid multiplier leverages the parallelism and efficiency of Vedic mathematics, particularly the Urdhva-Tiryagbhyam sutra, to improve partial product generation and reduce propagation delay. The use of reversible logic gates ensures minimal information loss, which contributes to reduced power dissipation making the design suitable for low-power VLSI applications. Furthermore, the Han-Karlson adder, with its logarithmic carry computation structure, accelerates addition operations and enhances overall throughput. This paper outlines the design methodology, logic-level implementation, and performance analysis of the proposed MAC architecture. The system is modelled using Hardware Description Language (HDL) and simulated using Xilinx ISE 14.7 (AMD-compatible version) within a virtualized environment on Oracle VirtualBox. Performance metrics such as delay, power consumption, and area utilization are evaluated and compared against conventional MAC architectures. The simulation results indicate notable improvements, especially in speed and power efficiency, making the proposed MAC unit highly suitable for integration into next-generation DSP processors, AI accelerators, and embedded computing platforms.

II. LITERATURE REVIEW

[1] Thapliyal, H., & Srinivas, M. B. (2005) This paper presents the design of reversible logic-based multipliers using reversible gates like Fredkin and Toffoli.

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Impact Factor 8.066 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 12, Issue 5, May 2025

DOI: 10.17148/IARJSET.2025.12502

The study shows that reversible logic can reduce energy dissipation and is suitable for low-power VLSI systems. The multiplier designs are evaluated based on the number of gates, garbage outputs, and quantum cost.

[2] Kirthiga, R., & Vijayalakshmi, P. (2010) This work introduces a high-speed MAC unit using Vedic multipliers. The Urdhva Tiryagbhyam sutra is employed to improve multiplication speed. Implementation on FPGA shows better area and speed trade-offs compared to conventional multipliers, validating the use of Vedic methods for signal processing hardware.

[3] Kaur, M., & Kaur, R. (2014) This study implements an efficient Booth multiplier using modified encoding to reduce partial product generation. Targeted for DSP applications, the design reduces critical path delay and power consumption. Simulations in Xilinx ISE confirm improvements in speed and area.

[4] Sultana, R., & Hossain, M. M. (2018) The paper introduces a hybrid multiplier combining Vedic and Booth algorithms to exploit the advantages of both. The approach reduces partial product count while maintaining parallel computation. Results on Spartan-6 FPGA indicate enhanced performance in terms of speed and resource usage.

[5] Kumari, R., & Sharma, S. (2021) This study proposes an optimized Han-Carlson adder for use in high-performance arithmetic circuits. By adjusting the black and gray cell structures, the adder achieves reduced delay and area. The adder is integrated into a MAC unit and tested on Virtex-7 FPGA for timing and power metrics.

[6] Patel, S., & Mehta, P. (2023) A recent work focusing on a reversible logic-based MAC unit using a combination of hybrid multipliers and efficient adders. The design integrates Booth and Vedic multipliers along with reversible logic gates like Peres and Feynman to enhance energy efficiency. Simulations on Vivado demonstrate low-power operation and high-speed performance.

III. EXISTING METHOD

The existing method for designing a 32-bit MAC unit uses a Vedic multiplier based on the Urdhva Tiryagbhyam sutra and reversible logic gates to achieve higher speed, reduced area, and lower power consumption. The Vedic multiplier minimizes partial product generation, reducing critical path delay and improving performance over conventional designs. Reversible logic gates like the DKG gate ensure minimal power dissipation by avoiding information loss, making them suitable for low-power and quantum computing applications. The architecture integrates the multiplier, reversible logic-based adder, and accumulator to complete MAC operations efficiently. Implemented using Verilog HDL and synthesized in Cadence RTL Compiler and Xilinx, the design shows improved delay, power, and area metrics compared to traditional MAC units.

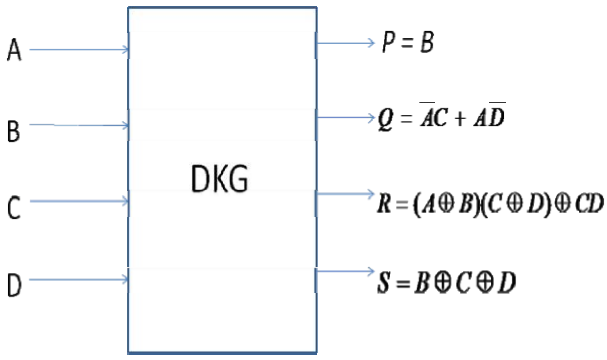

Fig 1: DKG gate as a Full adder

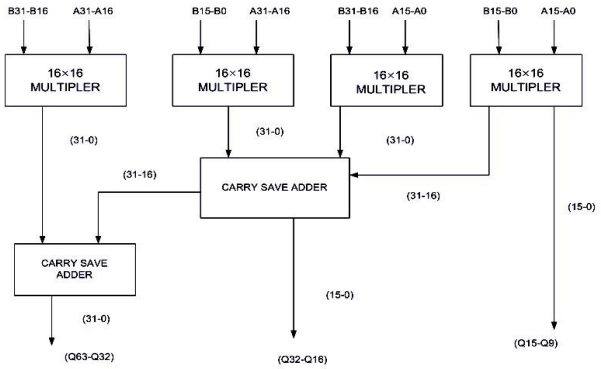

Fig 2: 32 × 32 Vedic Multiplier with Carry save Adder

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Impact Factor 8.066 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 12, Issue 5, May 2025

DOI: 10.17148/IARJSET.2025.12502

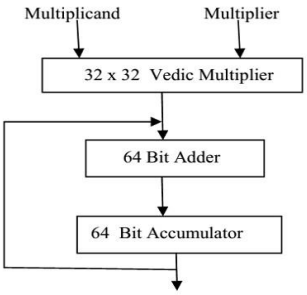

Fig 3: MAC unit Architecture

RESULTS

RTL Schematic

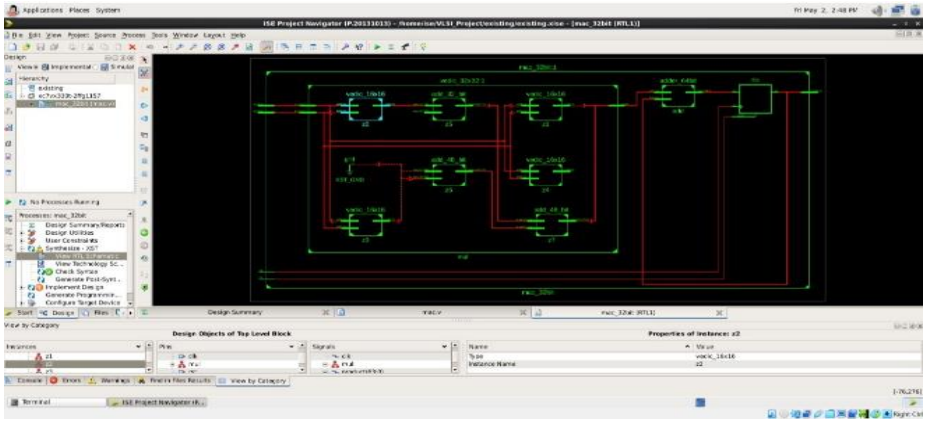

Fig 4: RTL Schematic of Existing Method

Timing Waveform

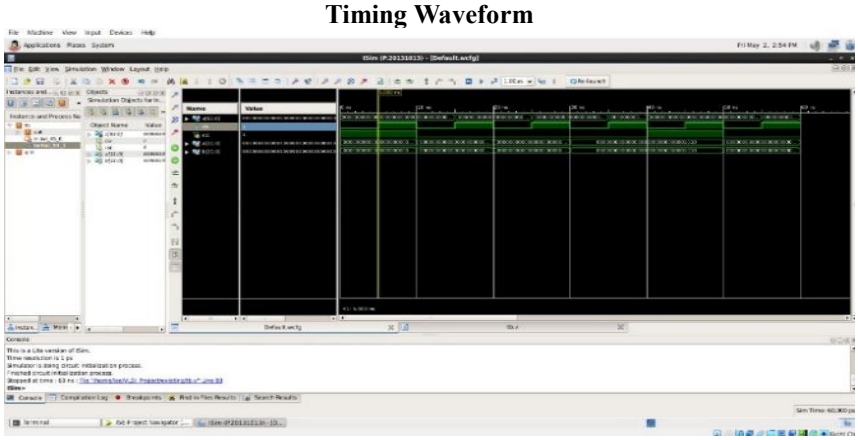

Fig 5: Timing Waveform of Existing Method

IV. PROPOSED METHOD

1. A 32-Bit MAC Unit using Hybrid Multiplier with Reversible logic gates and Han-Carlson adder

The proposed 32-bit MAC unit combines Vedic and Booth multipliers to form a hybrid multiplier that reduces partial products and improves speed. The multiplication result is added to the previous output using an adder designed with reversible DKG gates to minimize power dissipation. A Han-Carlson adder is used to perform fast and efficient addition with low delay. Vedic multiplication provides high-speed parallel processing, while Booth encoding effectively handles signed numbers. Reversible logic ensures no information loss and low energy consumption. The MAC unit consists of three main parts: multiplier, reversible adder, and accumulator. This design achieves better performance in terms of speed, area, and power. It is well-suited for applications in signal processing and embedded systems. The overall architecture is efficient and optimized for modern low-power computation.

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Impact Factor 8.066 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 12, Issue 5, May 2025

DOI: 10.17148/IARJSET.2025.12502

2. Block Diagram

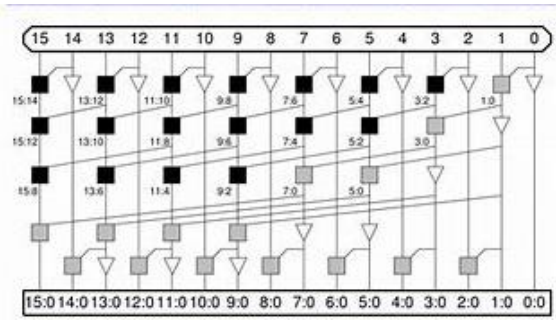

Fig 6: Han-Carlson adder

3.Software Tool (Xilinx ISE 14.7)

In the project titled "A 32-bit MAC Unit Design Using Hybrid Multiplier with Reversible Logic Gates and Han-Carlson Adder", Xilinx ISE 14.7 serves as the primary software tool for the development, simulation, synthesis, and implementation of the VHDL-based design. It facilitates the entry and management of modular VHDL code, allowing the design of individual components such as the hybrid multiplier (which combines Vedic and Booth techniques), the Han-Carlson adder, and the reversible logic gates. The software provides simulation capabilities through its integrated ISim tool, enabling functional verification of each module and the overall MAC unit. Furthermore, Xilinx ISE 14.7 supports synthesis and timing analysis, optimizing the logic for the targeted FPGA device, and generating a bitstream for implementation. The design hierarchy, signal tracing, and waveform analysis features of ISE 14.7 help in debugging and ensuring correct operation of the 32-bit MAC unit. Ultimately, this tool plays a crucial role in validating the performance and resource efficiency of the proposed architecture in real hardware environments

V. RESULT

RTL Schematic

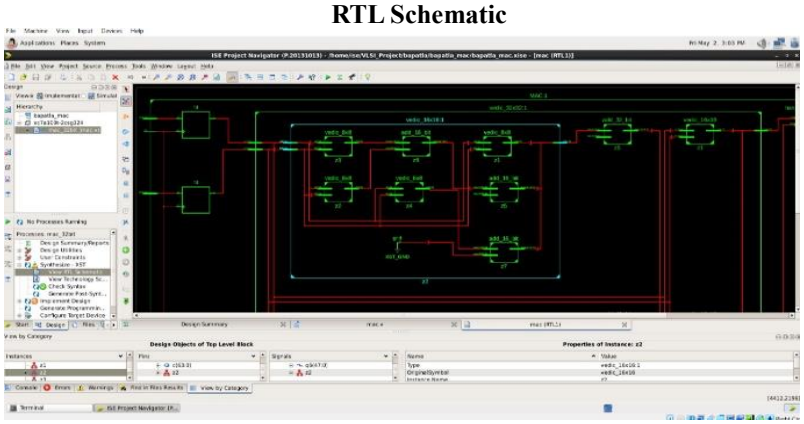

Fig 7: RTL Schematic of Proposed Method

Timing Waveform

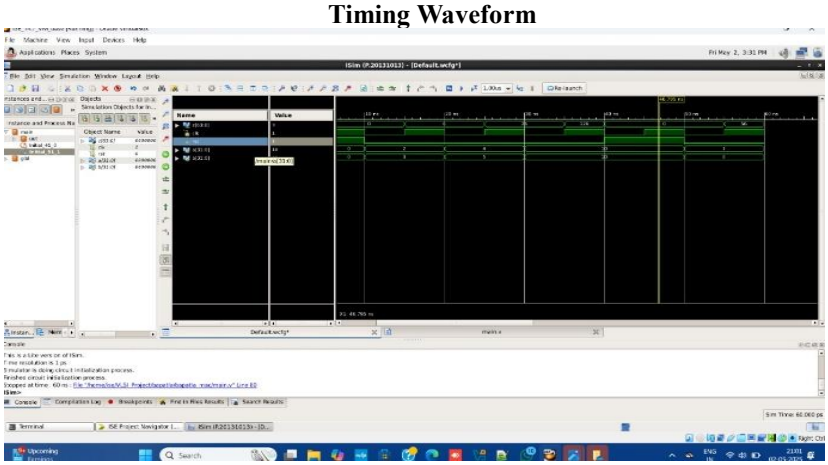

Fig 8: Timing Waveform of Proposed Method

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Impact Factor 8.066 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 12, Issue 5, May 2025

DOI: 10.17148/IARJSET.2025.12502

VI. CONCLUSION

In this project, a 32-bit MAC unit was successfully designed using a hybrid multiplier, reversible logic gates, and a Han-Carlson adder. The proposed architecture achieved improvements in speed, area, and power efficiency compared to traditional MAC units. By combining advanced multiplication and addition techniques with reversible logic, the design is highly optimized for modern low-power applications. Overall, the project demonstrates an effective approach for building high-performance arithmetic units.

VII. FUTURE SCOPE

The future scope of the project titled "A 32-bit MAC Unit Design Using Hybrid Multiplier with Reversible Logic Gates and Han-Carlson Adder" is significant, particularly in the fields of low-power, high-performance computing and quantum computing. The integration of reversible logic gates offers a foundation for energy-efficient computation, aligning with the growing demand for green and sustainable hardware solutions. This design can be further extended to higher bit-width operations (e.g., 64-bit or 128-bit) for use in advanced digital signal processing (DSP) systems, machine learning accelerators, and embedded processors. Additionally, the modular architecture allows for easy scalability and adaptation into application-specific integrated circuits (ASICs) or system-on-chip (SoC) designs.

REFERENCES

[1]. Sudhakar S.M., Chidambaram K.P., Swartzlander Jr E.E., (2012), “Hybrid Han-Carlson Adder”, Proceedings of the IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 818–821.Pratyusha Pushadapu, M. Shiva Kumar, (2024) “Analysis of A L-shaped Patch Antenna for 5G Applications, IJMOT-2024-5-352759, Vol.19, no.4, July 2024.

[2]. P. Michael Preetam Raj, Bhaskaruni Sandeep, D. Sai Mallik Reddy, P. Ramanjaneyulu, Sakhamuri Sai Pravallika, (2016), “Design of Prefix Adder Amalgamation Reversible Logic Gates using 16 Bit Kogge Stone Adder”,

[3]. P. SivaNagendra Reddy, M. Saraswathi, (2017), “Design and Implementation of FPGA based 64-bit MAC Unit using VEDIC Multiplier and Reversible Logic Gates”, Indian Journal of Science and Technology, Vol. 10, No. 3, pp. 1–8.

[4]. K. Kotiratnam, B. Ramu, (2017), “A 32 BIT MAC Unit Design Using Vedic Multiplier and Reversible Logic Gates”, International Journal & Magazine of Engineering, Technology, Management and Research (IJMETMR), February 2017.

[5]. S. A. Yuvaraj, K. Gunasekaran, D. Muthukumaran, K. Umapathy, (2018), “FPGA Implementation of Parallel Adder Using Reversible Logic Gates”, Micro-Electronics and Telecommunication Engineering, Lecture Notes in Networks and Systems, Vol. 179, Springer, Singapore, pp. 429–435.

[6]. H. Sai Ram Vamsi, K. Srinivasa Reddy, C. Babu, N.S. Murty, (2018), “Design of Reversible Logic Based 32-Bit MAC Unit Using Radix-16 Booth Encoded Wallace Tree Multiplier”, International Conference on Computer Communication and Informatics (ICCCI 2018), IEEE Xplore, 2018.

[7]. K. K. Reddy, M. S. Reddy, (2019), “Modified Han Carlson Adder Based Multiply Accumulate Unit for High Speed DSP Applications”, International Journal of Innovative Technology and Exploring Engineering (IJITEE), Vol. 8, Issue 6, April 2019.

[8]. Samraj Daphni, Kasinadar Sundari Vijula Grace, (2019), “Design and Analysis of 32-Bit Parallel Prefix Adders for Low Power VLSI Applications”, Advances in Science, Technology and Engineering Systems Journal, Vol. 4, No. 2, pp. 102–106.

[9]. B.S. Apoorva, M.A. Amjad, O. Bharatha, P.S. Surya, S. Nagendra Prasad, (2020), “Design of MAC Unit for an Artificial Neural Network Using Reversible Logic Gates”, Intelligent Computing Techniques for Smart Energy Systems, Lecture Notes in Electrical Engineering, Vol. 862, Springer, Singapore, pp. 297–308.

[10]. H.G. Rangaraju, U. Venugopal, K.N. Muralidhara, K.B. Raja, (2020), “Low Power Reversible Parallel Binary Adder/Subtractor”, arXiv preprint arXiv:1009.6218.

[11]. Rakshith Saligram, Shrihari Shridhar Hegde, Shashidhar A. Kulkarni, H.R. Bhagyalakshmi, M.K. Venkatesha, (2020), “Design of Parity Preserving Logic Based Fault Tolerant Reversible Arithmetic Logic Unit”, arXiv preprint arXiv:1307.3690.

[12]. H.R. Bhagyalakshmi, M.K. Venkatesha, (2020), “Optimized Reversible BCD Adder Using New Reversible Logic Gates”, arXiv preprint arXiv:1002.3994.

[13]. M. Aditya, Y.B. Nithin Kumar, M.H. Vasantha, (2020), “Reversible Full/Half Adder with Optimum Power Dissipation”, 10th International Conference on Intelligent Systems and Control (ISCO), IEEE, pp. 1–4.

[14]. S.M. Swamynathan, V. Bhanumathi, (2020), “Design of Reversible Logic Based Full Adder in Current-Mode Logic Circuits”, Microprocessors and Microsystems, Vol. 79, Article 103100.

DOI: 10.17148/IARJSET.2025.12502

[15]. Anju Anna Wilson, Sreenidhi Prabha Rajeev, (2023), "Implementation of an Array Multiplier Using an Addition Algorithm with Signed Digit Representation", Proceedings of the 2023 International Conference on Computing, Communication, and Intelligent Systems (ICCCIS), IEEE, August 2023.

[16]. A. Radha, S. Maheswari, (2023), "High Speed Efficient Multiplier Design using Reversible Gates", International Journal of Engineering and Advanced Technology (IJEAT), Vol. 12, Issue 3, February 2023.

[17]. S. K. Sharma, R. K. Singh, (2023), "Design and Implementation of 32-bit MAC Unit Using Reversible Logic Gate", International Journal of Engineering Research & Technology (IJERT), Vol. 12, Issue 5, May 2023.

[18]. P. S. Reddy, M. Saraswathi, (2023), "FPGA Implementation of Multiplier-Accumulator Unit using Vedic Multiplier