IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology
International Conference on Interdisciplinary Global Research in Adaptation, Transformation & Engineering
INTEGRATE 2025
Geetanjali Institute of Technical Studies (GITS)

Vol. 12, SPECIAL ISSUE 2, NOVEMBER 2025 DOI: 10.17148/IARJSET/INTEGRATE.2025.12261

Neuromorphic Communication Systems: Bridging Brain-Inspired Computing and Wireless Networks

Arti Sharma[1], Shubham Teli [2], Mustansir Bohra[3], Vijay Kumar Gautam[4]

Professor, Department of Electronics and Communication Engineering, GITS, Udaipur (India)[1]

Students, Department of Electronics and Communication Engineering, GITS, Udaipur[2, 3, 4]

Abstract: Neuromorphic computing signals a paradigmatic shift toward processing, inspired by biological neural networks for efficient energy usage [1],[3],[10], adaptability, and learning information in real time. Instead of synchronous, clock-driven architectures that normally characterize the design of most traditional digital systems with separated memory and processing, neuromorphic systems employ asynchronous, event-driven SNNs [2], which integrate computation and memory. This significantly reduces the energy bottlenecks and allows low-power, scalable architectures. SNNs and event-driven frameworks are also expected to be indispensable components in ISAC, enabling efficient, adaptive information exchange in wireless networks, radar, and IoT or edge computing applications by allowing context- aware real-time processing with minimum redundant computation.

This review provides an overview of state-of-the-art neuromorphic architectures, sensors, and communication models, focusing on recent advances, hardware implementations, applications, and future challenges for the creation of truly intelligent and power-efficient communication systems.

Index terms: Neuromorphic Computing, Spiking Neural Networks (SNNs), Event-Driven Architecture Integrated Sensing and Communications (ISAC), Low Power Energy Efficiency, Neuromorphic Radar and Wireless Sensing, Edge Computing and IoT Applications, Brain-Inspired Communication Systems, Spike-Timing Dependent Plasticity (STDP),

I. INTRODUCTION

Neuromorphic communication is inspired by how brains works and how machines process and exchange information in a way that Traditional computers keep memory and processing separate and run everything in a cycle [1],[5]. Neuromorphic systems throw this away, bringing these pieces together and copying nature's approach. The payoff is huge—way less power consumption and incredible flexibility when environments change. This matters a lot for battery- powered gadgets, mobile tools, and sensor networks scattered everywhere. The real magic comes from spiking neural networks (SNNs). Instead of smooth signals like ordinary AI, SNNs send bursts of electrical pulses, just like real neurons do. They only spring to life when something worth paying attention to happens, making them incredibly economical. These matters for wireless systems, radars, and edge devices because they desperately need instant responses and smart resource management. Neuromorphic systems solve this by tightening connections and cutting down pointless data. Learning happens through spike-timing dependent plasticity (STDP), where connection strengths shift based on signal timing. This lets systems get smarter and more capable as they work. Our review covers the fundamentals, latest breakthroughs in hardware and sensors, real applications from cities to robots, and real obstacles researchers face today. The research performed in this paper makes a systematic review of the Biological and Computational Foundation, Hardware Architecture, and Integrated Sensing and Communication (ISAC) about Neuromorphic Communication. To analyses and compare existing work about the development of Neuromorphic communication, the following data and figures are as follows.

II. BIOLOGICAL AND COMPUTATIONAL FOUNDATION

a. History of Biological and Computational Foundation

The paper explores the use of Neuromorphic Computing for low power edge inference within the IoT. Carver Mead introduces the concept in 1980s to design an electronic device that mimic the structure and function of biological neural network [10]. In early 2000s the concept of computational neuroscience and neuromorphic hardware was introduced model like HODGKIN-HUXLEY, IZHIKEVICH AND LEAKY INTEGRATE AND FIRE (LIF) became standard neuron model linking with which in 2010s Neuromorphic chips emerged (e.g. IBM TrueNorth, Intel Loihi) demonstrated brain like parallel processing. Around this time, researchers began applying neuromorphic vision to communication system focusing on low latency, low power and adaptive communication. In late 2010s – Early 2020s the field evolved into Neuromorphic communication. In Modern Era Neuromorphic communication principle is applied in 5G/6G network, (ISAC), Adaptive modulation and coding using SNNs.

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology
International Conference on Interdisciplinary Global Research in Adaptation, Transformation & Engineering
INTEGRATE 2025
Geetanjali Institute of Technical Studies (GITS)

Vol. 12, SPECIAL ISSUE 2, NOVEMBER 2025 DOI: 10.17148/IARJSET/INTEGRATE.2025.12261

b. Biological Basis of Neuromorphic Communication

Neuromorphic Communication is directly inspired by human brain process and transmit the information. At the microcircuit level, neuronal cells are morphologically arranged in layers with various connectivity motifs. Using "analysis by synthesis" approach, engineers enhance electronic circuit through brain microcircuit. Mixed-signal implementations are more realistic than computer simulations or purely digital implementations [2][3]. Owing to the thermal noise in silicon, analog neuron circuits inherently generate stochastic spikes, similar to neuronal cells, where noise from ion channels and intrinsic neurotransmitter release results in stochastic spiking. His aim was to transfer this concept into electronic device which further demanded it for communication purpose.

c. ***Computational* Models and Architecture**

The SNN mimics biological neurons that independently process and forward spikes. a biologically inspired paradigm known as neuromorphic computing has been developed that behaves in a manner similar to the brain in both being parallel and being event-based. Neuromorphic processors use Spiking Neural (SNNs), where the transmission of information is spike-related for advanced exchange. This is in contrast to conventional processors which consume energy on each clock cycle whether input tasks change or do not change, making neuromorphic systems consume only power when an event occurs which in turn makes them far more energy give a level as well as allowing a neuromorphic system to execute a task instantly and in real-time even with very limited number of resources. With this asynchronous working mechanism, only a small subset of neurons is activated during inference. In essence, an SNN is inherently efficient in terms of computation.

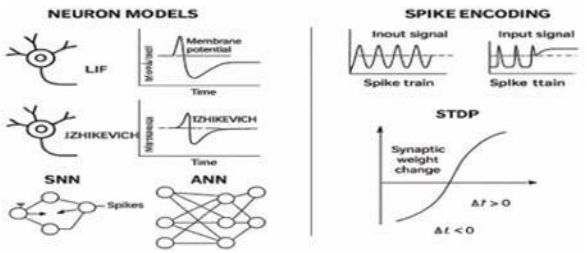


Figure .1

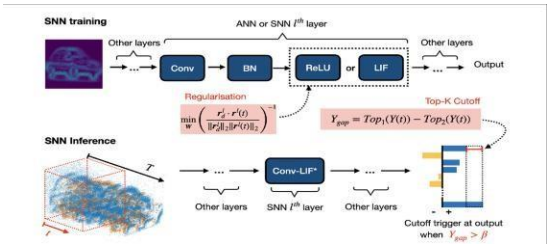


figure .2

Spiking neural networks (SNNs) have gained attention to their energy efficiency and low latency [1][2][3][8]. There are neuromorphic chips, such as Loihi and TrueNorth on which SNN can be deployed. Spike-timing-dependent plasticity (STDP) is an unsupervised brain-like learning rule implemented in many SNNs and neuromorphic chips. The performance of STDP learning in neuromorphic chips deteriorates because the resolution of synaptic efficacy in such chips is generally restricted to 6 bits or less. SNN mimics biological neurons that independently process and forward spikes. With this asynchronous working mechanism, only a small subset of neurons is activated during inference. In essence, an SNN is inherently efficient in terms of computation. an additional encoding step, such as rate-based coding and Poisson's code, is necessary for frame-based input before forward propagation in the SNN. One approach to train as SNN is through ANN-to-SNN conversion, which leverages the mature training regime of the ANN to first train a high- accuracy ANN and then convert it into an SNN. The proposed method has led to research focused on achieving near-zero conversion loss. Another methodology involves the use of backpropagation in SNN training. Due to the non-differentiable nature of spiking, this approach requires the deployment of a surrogate gradient.

III. NEUROMORPHIC HARDWARE ARCHITECTURE

a. Chip Design and Event-Driven Hardware

Neuromorphic Hardware architectures are designed to emulate the biological principle of the human brain through event driven and parallel computation. Several notable hardware platforms have been developed over the past decade. IBM'S TrueNorth chip mimics the structure and function of the human brain; it contains 4096 cores, each simulating 256 neurons and 256 million synapses [7]. This chip operates on event driven and non von Neumann architecture, where computation and memory are collocated to reduce power consumption (around 65mW). Intel's Loihi future advance this concept with programmable spiking neurons which combine many asynchronous Neurocore's, to support real time, lower power event computation, Loihi system have demonstrated large energy and speed gain on select edge and optimization workload. SpiNNaker platform is designed for real time execution, large scale simulation of spiking neural network. Its building block is an 18- core ARM968 SoC. Many such chips are tiled in rack to form the million-core machine capable of simulating brain scale network. It routes spikes as small multicast packets through a custom packet switched network and runs PyNN models via the sPyNNaker/SpiNNTool toolchain.

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

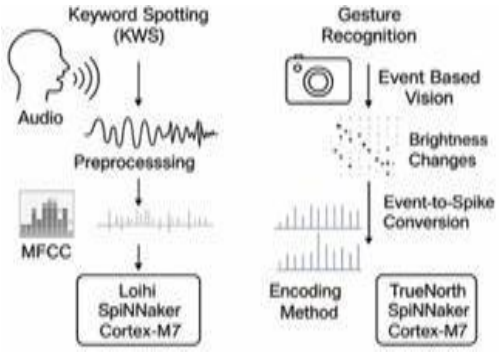
International Advanced Research Journal in Science, Engineering and Technology
International Conference on Interdisciplinary Global Research in Adaptation, Transformation & Engineering
INTEGRATE 2025
Geetanjali Institute of Technical Studies (GITS)

Vol. 12, SPECIAL ISSUE 2, NOVEMBER 2025 DOI: 10.17148/IARJSET/INTEGRATE.2025.12261

Platform	Core Type	Learning Support	Processing Model	Application Suitability
Intel Loihi	Digital (128 cores)	On – chip STDP (online)	Event – driven, asynchronous	Adaptive edge-AI, real- time learning
IBM TrueNorth	Digital (1M neurons)	None (inference only)	Synchronous, fixed routing	Static low- power inference task
SpiNNaker (4C)	Digital (ARM 9 cores)	Software- based (offline)	Packet – based, parallel SNN sim	Flexible simulation, research system
STM32 Cortex-M7(MCU)	Von Neumann (ANN-based)	No	Frame – based feedforward ANN	General purpose low power edge AI

b. Analog and Mixed- Signal Approaches

Neuromorphic architecture also explores analog and mixed signal approaches to closely replicate biological neuron and synapse behavior. Analog design implement neurons/synapse
dynamic as continuous time/subthreshold circuits with very low power and high density, typical architecture pattern compute in analog (dendrite/synapse circuit), encode spikes as digital address event send them across a packetized/event network and handle control in the digital domain. Mixed signal system combines analog neuron/synapse computation with digital event routing and control, mixing in digital event-based communication gives scalable, asynchronous interconnect and configurability



c. Focus on Low Power and Energy Efficiency

The central feature of this system is energy efficiency achieved through event driven signaling where computation occur only upon neural spike event drastically reducing power consumption. Comparative studies shows that chips like loihi can achieve up to thousand-fold improvement in energy efficiency over conventional CPU- based implementation, making them highly suitable for low latency.

IV. INTEGRATED SENSING AND COMMUNICATION (ISAC)

Neuromorphic principle in ISAC aims to merge the function of sensing and date transmission into a unified framework, reducing system redundancy and energy use [5]. ISAC system performs sensing and data exchange simultaneously, improving latency and power efficiency. Neuromorphic principle in ISAC aims to merge the function of sensing and date transmission into a unified framework, reducing system redundancy and energy use. Neuromorphic principle such as spike-based computation, local learning and event driven processing enables this integration efficiently. ISAC system performs sensing and data exchange simultaneously, improving latency and power efficiency. Traditional communication systems use continuous or periodic signal exchange, which wastes bandwidth and power. Neuromorphic ISAC adopts event driven communication where information is transmitted only when an event (spike or sensor change) detected similar to biological neurons mechanism. This model allows asynchronous, low latency data transfer and support distributed intelligence making it ideal for edge computing, autonomous system and IoT network.

V. NEUROMORPHIC RADAR AND WIRELESS SENSING

a. Introduction to Neuromorphic Radar Systems

Radar sensors are becoming common in IoT devices, often use a lot of power, which is a problem for devices which are dependent on battery and needed for a longer period of time. Many of these systems also use artificial neural networks (ANNs) to analyse signals which require continuous processing and frequent data transfers between the processor and memory. Radar-based IoT devices often face challenges in keeping power consumption low. Recent advances in neuromorphic engineering have in

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology
International Conference on Interdisciplinary Global Research in Adaptation, Transformation & Engineering
INTEGRATE 2025
Geetanjali Institute of Technical Studies (GITS)

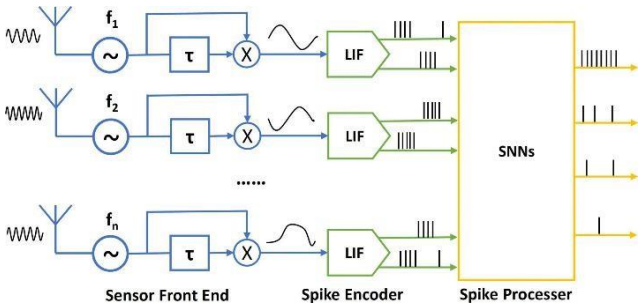
Vol. 12, SPECIAL ISSUE 2, NOVEMBER 2025 DOI: 10.17148/IARJSET/INTEGRATE.2025.12261

spired spiking neural networks (SNNs) and dedicated neuromorphic circuits that better approach the efficiency of sensory signal processing in the brain.

Most current SNN-based radar systems don't use a complete neuromorphic hardware design. Their front-end circuits still work like traditional radars, using much more power—often in the tens or hundreds of milliwatts—while the neuromorphic processing itself only uses a few hundred microwatts. This paper proposes NeuroRadar—a fully neuromorphic radar system. It takes inspiration from biological sensing, producing event-driven spikes only when motion is detected instead of continuously sending data. NeuroRadar integrates the sensing and spiking computation together in one architecture for lower power use and faster, more efficient sensing.

b. Hardware Architectures for Neuromorphic Radar

NeuroRadar consists of three main components: sensor front end, spike encoders, and spike processors. The sensor front end senses ambient motion, and the output signals are converted into spike sequences (referred to as spike trains) by the spike encoders. These spike trains are then directly processed by the energy-efficient SNNs.



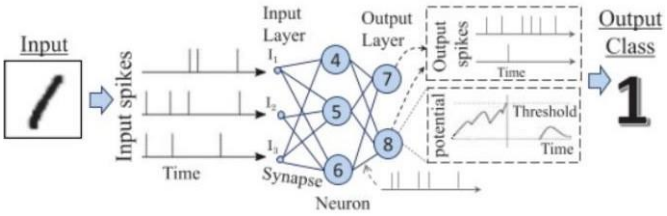
Sensor front-end: The NEURORADAR front-end emits a weak, continuous-wave single-tone signal in the 0.3∼3 GHz ultra-high frequency (UHF) band. The core component is a SILO whose frequency is modulated by the motion of the surrounding targets [90]. By demodulating this frequency shift, the system generates a base band signal that carries the motion information. We further introduce a sensor array design that combines multiple SILOs with different operating frequencies to provide richer spatiotemporal information

Spike encoder. The spike encoding circuit takes the baseband signal produced by the front-end and converts the signal into spike trains following the LIF model [5]. Given that the input is AC-coupled and the signal comprises both positive and negative parts, two spike encoders are jointly employed to encode each channel of the radar sensor. The spike encoding circuits operate entirely in an event-driven manner; they only generate spikes when the sensor front-end detects motion and stays idle otherwise.

Spike processor: The spike encoders interface directly with the neuromorphic computing circuits, enabling all signals to be pro cessed within the spike domain. Our approach involves designing multi-layer convolutional SNNs to process the multi-channel spike chains from the NEURORADAR sensor array. These SNNs execute pattern recognition and regression tasks according to the application requirements.

c. Event-Driven Wireless Sensing with Spiking Neural Networks

Spiking neural networks (SNNs) mimics biological neurons that independently process and forward spikes. With this asynchronous working mechanism, only a small subset of neurons is activated during inference. In essence, an SNN is inherently efficient in terms of computation**.** Biological neurons exchange information through the generation and transmission of electrical impulses, often referred to as spikes. These neurons are connected to one another through specialized junctions known as synapses. A neuron emits a spike when the incoming signals, gathered together, elevate its membrane potential beyond a specific threshold, after which it resets. This mechanism is typically modelled using the Leaky-Integrate-and-Fire (LIF) framework.[15][19]. In conventional artificial neural networks (ANNs), information is represented through continuous real-valued activations, where functions like ReLU approximate the firing rates of biological neurons. [15][19]



IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology
International Conference on Interdisciplinary Global Research in Adaptation, Transformation & Engineering
INTEGRATE 2025
Geetanjali Institute of Technical Studies (GITS)
Vol. 12, SPECIAL ISSUE 2, NOVEMBER 2025 DOI: 10.17148/IARJSET/INTEGRATE.2025.12261

VI. EDGE COMPUTING AND IOT INTEGRATION

These systems, stimulated by biological processes, let sensors process data at the edge with very little power, which cuts down on both latency and bandwidth needs. Neuromorphic sensors work like the human sensory system by being able to detect and process events in real time. This method makes it possible to keep an eye on things all the time and make decisions that change based on the situation in a number of IoT applications, such as environmental sensing, industrial automation, and healthcare monitoring. Neuromorphic computing helps make human-robot interaction systems more advanced, which makes it easier for people and machines to work together.

a. Important Advantages of Neuromorphic Chips

- Because of their event-driven architecture, neuromorphic chips use only 1% to 10% of the power that traditional processors do.[7][8]
- Event-driven processing: neuromorphic chips only turn on when they need to, just like a motion sensor turns on a light when it sees movement. This cuts down on energy use that isn't needed.
- Example: IBM's TrueNorth chip reduced energy consumption by 98% in DARPA's autonomous robotics trials by eliminating redundant data transfers

b. ***Real time and on device processing:*** The study of IJFMR show that AI Neuromorphic architectures are more than capable of real-time processing because they emulate the parallel, asynchronous dynamics of biological neurons. The results of Lin et al. (2021) show that a reduction of more than 50 percent in inference latency of ultra-small edge accelerators with neuromorphic integration compared to conventional CNN accelerators achieves real-time vision recognition.
Example: Prophesee's event-based vision sensors, when paired with Sony's neuromorphic chips, detect pedestrians 20ms faster than conventional frame-based cameras—a critical advantage for autonomous vehicles navigating urban environments.[6]

c. Market availability or practical applications:

Company	Flagship product	Commercial launch	Product deployment
Brainchip	Akida NSoC	2024(pre -orders)	Edge ai box
Intel	Loihi 2	2021(announce)	Sandia labs hala point
synSense	Speck	2023	Vision processor demo kit
Prophesee	GenX320 sensor	2023	Edge ai devices

VII. LEARNING AND ADAPTATION MECHANISMS

spike time-dependent plasticity (STDP) is the most well-known learning rule for unsupervised learning in the brain, which is implemented in many neuromorphic systems. The STDP algorithm modulates the weight of a synapse based on the relative timing of the pre- and post-synaptic spikes. The weight of a synapse will be increased if a pre-synaptic spike arrives several milliseconds before the post-synaptic spike fires. On the other hand, the weight will be decreased in the case that the post-synaptic spike fires earlier than the arrival of a pre-synaptic spike by several milliseconds. The amount and direction of alteration of the weight are determined by the time between the arrival of the pre- and post-synaptic [5] spike [2][3][4][13][14].
STDP-based unsupervised learning has been successful in tasks such as pattern detection (Masquelier et al., 2008, 2009) and image classification (Diehl and Cook, 2015), achieving high performance in simulation.

a. ***Adaptive STDP learning****:* When using the STDP learning, the network dynamics evolve as follows. The spike inputs received via synapses cause the neuron to spike. If the input spike (presynaptic spike) activating a synapse arrives before the postsynaptic spike (if the synapse contributes to the spiking of the neuron), the value of its synaptic weight is potentiated. On the other hand, if the input spike (presynaptic spike) activating the synapse arrives after the postsynaptic spike (if the synapse does not contribute to the spiking of the neuron), the value of its synaptic weight is depressed. The closer the pre-and the postsynaptic spikes are to each other, the higher is the value of potentiation or depression SNNs that use STDP for processing automotive radar are very adaptable to changing traffic conditions. They can still track targets accurately in situations where the traffic is not stationary, and they use orders of magnitude less power than traditional methods. Like this, memristor-based adaptive neuromorphic systems let autonomous systems work in uncertain wireless environments switch contexts quickly without help from people. These systems can update their awareness in about 1 millisecond.[2][3]

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology
International Conference on Interdisciplinary Global Research in Adaptation, Transformation & Engineering
INTEGRATE 2025
Geetanjali Institute of Technical Studies (GITS)

Vol. 12, SPECIAL ISSUE 2, NOVEMBER 2025 DOI: 10.17148/IARJSET/INTEGRATE.2025.12261

VIII. CHALLENGES AND FUTURE DIRECTIONS

Neuromorphic communication is hugely promising, but several key challenges remain that must be overcome before it can achieve widespread commercial deployment. Among these, scalability poses one of the biggest hurdles: building large, robust networks that retain efficiency in their functionality as size and complexity increase is non-trivial. Integration with existing digital communication technologies in turn poses a major technical barrier, as neuromorphic hardware and protocols diverge significantly from mainstream approaches. Because hardware parts can vary, some devices aren't always reliable, and there aren't any common standards yet, it becomes hard to build and program these systems on a large scale [9]. Another important point is that the current learning algorithms, like STDP, for SNNs need to be modified and optimized for real-world heterogeneous data streams.[5]

On the positive side, continuous efforts are being devoted to optimizing algorithm-hardware co-design, hybrid analog- digital circuits, and adaptive event-driven architectures in order to mitigate these bottlenecks. Some promising trends involve the employment of memristive devices for efficient synaptic implementation, neuromorphic chip adoption in edge AI and IoT, and exploring ASICs exclusively devoted to low-power communications. As more and more commercial players start investing in this domain, along with demonstration projects at validating practical use cases, neuromorphic communication is on a promising trajectory toward mainstream adoption.

IX. CONCLUSION

Neuromorphic communication at its core is redefining how intelligent machines sense, process, and share information by combining biology-inspired principles with state-of-the-art engineering. The field represents an unprecedented approach toward ultra-low-power, adaptable, and effective data exchange that is essential for future IoT, smart infrastructure, and next-generation wireless networks. Even though there are still many technical hurdles when it comes to scaling, integration, and creating common standards, the rapid progress in research and emerging hardware shows a lot of promise. As technology has evolved, neuromorphic communication has the potential to completely transform how intelligent and energy-efficient communication systems function.[7] [8] [9]

REFERENCES

[1] B. Vogginger, F. Kreutz, J. López-Randulfe, C. Liu, R. Dietrich, H. A. Gonzalez, D. Scholz, N. Reeb, D. Auge, J. Hille, M. Arsalan, F. Mirus, C. Grassmann, A. Knoll, and C. Mayr, "Automotive radar processing with spiking neural networks: Concepts and challenges," *Frontiers Neurosci. *, vol. 16, p. 851774, Apr. 2022, doi: 10.3389/fnins.2022.851774.

[2] A. Gautam and T. Kohno, "Adaptive STDP-based on-chip spike pattern detection," *Frontiers Neurosci. *, vol. 17, p. 1203956, Jul. 2023, doi: 10.3389/fnins.2023.1203956.

[3] A. Gautam and T. Kohno, "An adaptive STDP learning rule for neuromorphic systems," *Frontiers Neurosci. *, vol. 15, p. 741116, Sep. 2021, doi: 10.3389/fnins.2021.741116.

[4] G. Hennequin, W. Gerstner, and J. P. Pfister, "STDP in adaptive neurons gives close-to-optimal information transmission," *Frontiers Comput. Neurosci. *, vol. 4, p. 143, Dec. 2010, doi: 10.3389/fncom.2010.00143.

[5] K. Zheng, A. Basu, E. Sacks, and J. Etienne, "NeuroRadar: A fully neuromorphic radar system," in *Proc. ACM SenSys*, 2023, pp. 1–14.

[6] S. K. Esser, R. Appuswamy, P. Merolla, J. V. Arthur, and D. S. Modha, "Convolutional networks for fast, energy-efficient neuromorphic computing," *Proc. Nat. Acad. Sci.*, vol. 113, no. 41, pp. 11441–11446, Oct. 2016, doi: 10.1073/pnas.1604850113.

[7] P. A. Merolla, J. V. Arthur, R. Alvarez-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B. V. Jackson, B. A. Imam, C. Guo, Y. Nakamura, S. Brezzo,I. Vo, S. L. Esser, R. Appuswamy, B. Taba, A. Amir, M. D. Flickner, W. P. Risk, and D. S. Modha, "A million spiking-neuron integrated circuit with a scalable communication network and interface," *Science*, vol. 345, no. 6197, pp. 668–673, Aug. 2014, doi: 10.1126/science.1254642.

[8] M. Davies, N. Srinivasa, T. H. Lin, G. Chinya, Y. Cao, S. H. Choday, G. Dimou, H. Japes, A. Kusnitz, R. Lines, O. Liu, D. Mathaikutty, S. McCoy, A. Patel, A. Phillips, N. Redd, S. A. Shok, S. K. Sinha, D. Sinha, T. Sinha, J. Weng, and E. Wild, "Loihi: A neuromorphic manycore processor with on-chip learning," *IEEE Micro*, vol. 38, no. 1, pp. 82–99, Jan. 2018, doi: 10.1109/MM.2018.112130359.

[9] S. B. Furber, D. R. Galluppi, S. Temple, and L. A. Plana, "The SpiNNaker project," *Proc. IEEE*, vol. 102, no. 5, pp. 652–665, May 2014, doi: 10.1109/JPROC.2014.2304638.

[10] C. Mead, "Neuromorphic electronic systems," *Proc. IEEE*, vol. 78, no. 10, pp. 1629–1636, Oct. 1990, doi: 10.1109/5.58356.

[11] G. Indiveri, B. Linares-Barranco, T. J. Hamilton, A. van Schaik, R. Etienne-Cummings, T. Delbruck, S. C. Liu, P. Dudek, S. Häfliger, A.Jiménez-Fernández, S. Costas, R. Vincent, and T. C. Pearson, "Neuromorphic silicon neuron circuits," *Frontiers Neurosci. *, vol. 5, p. 73, Jun. 2011, doi: 10.3389/fnins.2011.00073.

[12] T. Masquelier, R. Guyonneau, and S. J. Thorpe, "Spike timing dependent plasticity finds the start of repeating patterns in continuous spike trains," *PLoS ONE*, vol. 3, no. 4, p. e1377, Apr. 2008, doi: 10.1371/journal.pone.0001377.

[13] G.-Q. Bi and M.-M. Poo, "Synaptic modifications in cultured hippocampal neurons: Dependence on spike timing, synaptic strength, and postsynaptic cell type," *J. Neurosci. *, vol. 18, no. 24, pp. 10464–10472, Dec. 1998, doi: 10.1523/JNEUROSCI.18-24-10464.1998.

[14] H. Markram, J. Lübke, M. Frotscher, and B. Sakmann, "Regulation of synaptic efficacy by coincidence of postsynaptic APs and EPSCs,"*Science*, vol. 275, no. 5297, pp. 213–215, Jan. 1997, doi: 10.1126/science.275.5297.213.

[15] W. Gerstner and W. M. Kistler, *Spiking Neuron Models: Single Neurons, Populations, Plasticity*. Cambridge Univ. Press, Cambridge, UK, 2002.

[16] E. M. Izhikevich and G. M. Edelman, "Large-scale model of mammalian thalamocortical systems," *Proc. Nat. Acad. Sci.*, vol. 105, no. 9, pp. 3593–3598, Mar. 2008, doi: 10.1073/pnas.0712231105.

[17] N. Qiao, H. Mostafa, F. Corradi, M. Osswald, F. Stefanini, D. Sumislawska, S. C. Liu, G. Indiveri, and R. Douglas, "A reconfigurable on-line learning spiking neuromorphic processor comprising 256 neurons and 128K synapses," *Frontiers Neurosci. *, vol. 9, p. 141, Apr. 2015, doi: 10.3389/fnins.2015.00141.

[18] J. Schemmel, D. Brüderle, A. Grübl, M. Hock, K. Meier, and S. Millner, "A wafer-scale neuromorphic hardware system for large-scale neural modeling," in *Proc. ISCAS*, 2010, pp. 1947–1950, doi: 10.1109/ISCAS.2010.5536970.

[19] T. Delbruck, V. Säckinger, C. A. Mead, and C. E. Fowler, "1000×1000 silicon retina," in *Digest of Technical Papers ISSCC*, 1991, pp. 188– 189, doi: 10.1109/ISSCC.1991.144321.

[20] S. J. Thorpe, A. Delorme, and R. Van Rullen, "Spike-based strategies for rapid processing," *Neural Networks*, vol. 14, no. 6–7, pp. 715–725, 2001, doi: 10.1016/S0893-6080(01)00083-1.

[21] W. Maass, "Networks of spiking neurons: The third generation of neural network models," *Neural Networks*, vol. 10, no. 9, pp. 1659–1671, 1997, doi: 10.1016/S0893-6080(97)00011-7.

[22] P. U. Diehl and M. Cook, "Unsupervised learning of digit recognition using spike-timing-dependent plasticity," *Frontiers Comput. Neurosci. *, vol. 9, p. 99, Aug. 2015, doi: 10.3389/fncom.2015.00099.

[23] T. Masquelier, R. Guyonneau, and S. J. Thorpe, "Competitive STDP-based spike pattern learning," *Neural Computation*, vol. 21, no. 5, pp. 1259–1276, May 2009, doi: 10.1162/neco.2008.06-08-804.

[24] J. P. Pfister and W. Gerstner, "Triplets of spikes in a model of spike timing-dependent plasticity," *J. Neurosci. *, vol. 26, no. 38, pp. 9673–9682, Sep. 2006, doi: 10.1523/JNEUROSCI.1425-06.2006.

[25] A. Kasinski and F. Ponulak, "Comparison of supervised learning rules for spiking neural networks," *Neurocomputing*, vol. 69, no. 13–15, pp. 1894–1903, Jun. 2006, doi: 10.1016/j.neucom.2005.12.110.

[26] J. P. Pfeil, T. Potjans, T. C. Schrader, S. Schemmel, M. Diesmann, and K. Meier, "Is a 4-bit synaptic weight resolution enough? Constraints on enabling spike-timing dependent plasticity in neuromorphic hardware," *Frontiers Neurosci. *, vol. 6, p. 90, Jun. 2012, doi: 10.3389/fnins.2012.00090.