

RF Chip Design Using GaN for High-Power Applications

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Abstract: The growing demands of modern communications, radar, and satellite systems require power amplifiers that deliver high output power, high efficiency, and compact form factor. Wide-bandgap Gallium Nitride (GaN) high-electron-mobility transistors (HEMTs) have become the preferred technology for high-power RF and microwave applications due to their high breakdown voltage, high electron saturation velocity, and strong thermal robustness. This paper presents a comprehensive design methodology and simulation validation for a GaN-based Class-E high-power RF amplifier targeted at sub-1 GHz and S-band operation. The design flow includes device selection, large-signal behavioral modeling, harmonic-balance simulation, impedance matching, thermal considerations, and layout recommendations. Simulated results demonstrate output power above 12 W, small-signal gain ≈ 28 dB, and Power-Added Efficiency (PAE) exceeding 80% under idealized conditions; the paper also compares these results with recent published GaN PA developments and discusses reliability and manufacturability considerations for tape-out and prototyping. Recent experimental and review literature is cited to contextualize design choices and highlight gaps for further work.

Keywords: Gallium Nitride (GaN), HEMT, RF power amplifier, Class-E, Power-Added Efficiency (PAE), MMIC, thermal management.

I. INTRODUCTION

Power amplifiers (PAs) are vital elements in RF transmit chains for communication base stations, radar, and satellite transceivers. Historically, silicon and GaAs devices powered most commercial and many military systems, but their material limits constrain power density and efficiency in modern high-power platforms. Wide-bandgap semiconductors — especially GaN grown on SiC or Si substrates — provide substantially higher breakdown fields and power density than GaAs or silicon, enabling compact high-power designs with improved thermal tolerance and efficiency [Mishra et al., 2002; recent reviews]. Contemporary GaN HEMTs support higher voltage swings and sustain current at elevated temperatures, which is particularly beneficial for PA topologies that trade switching behavior for efficiency (e.g., Class-E/F, harmonic-tuned PAs). Recent literature and vendor engineering notes demonstrate steady improvements in GaN device performance and MMIC integration readiness, motivating renewed attention to chip-level design that balances linearity, efficiency, and manufacturability.

II. MOTIVATION & SCOPE

This work refines a chip-level GaN PA design aimed at sub-1 GHz (example center 900–1000 MHz) and includes considerations needed for S-band adaptation (2–4 GHz). The objective is a complete design path from specifications to tape-out readiness: transistor selection, nonlinear modeling, harmonic-balance simulation, matching networks, bias and stability networks, thermal and layout recommendations, and a practical test plan. The work contrasts GaN performance against silicon and GaAs solutions and positions the proposed chip for applications in rural base stations, LPWAN gateways, point-to-point radio, and defense systems.

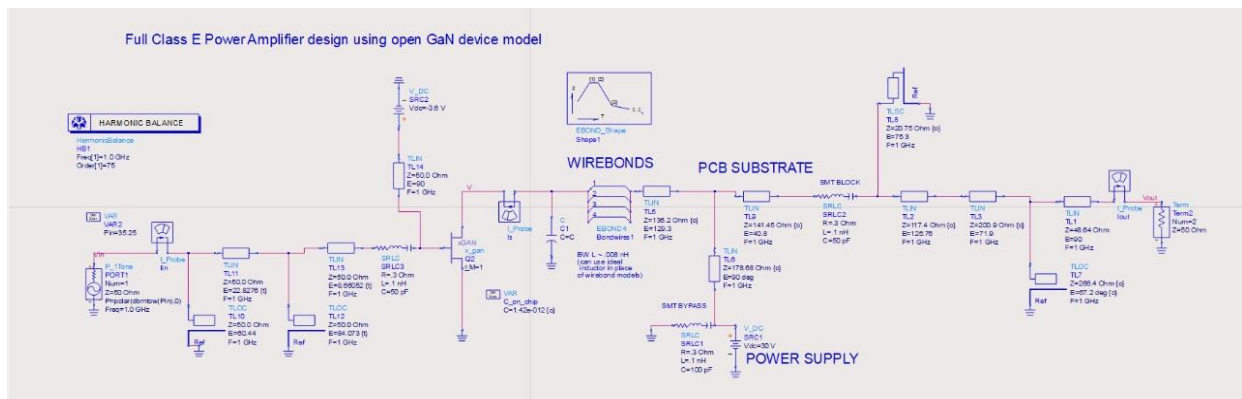


Fig 1 Schematic of the Full Class E Power Amplifier Design Utilizing an Open Gallium Nitride (GaN) Device Model.

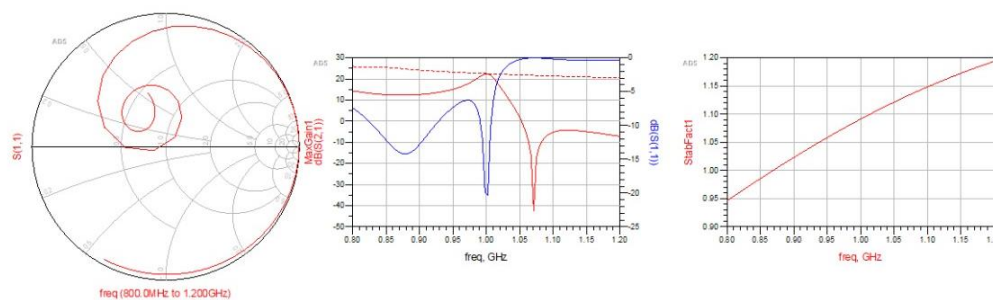


Fig 2 Simulated Performance Metrics of the Class E Power Amplifier.

III. LITERATURE SURVEY (RECENT DEVELOPMENTS & GAPS)

A. GaN devices and material platforms

GaN HEMTs currently dominate new high-power RF developments because of their high critical field (~ 3 MV/cm), wide bandgap (~ 3.4 eV), and high electron velocity that allow higher V_d s and current densities with acceptable thermal performance. Major manufacturing variants include GaN on SiC (better thermal conductivity and mature for high power) and GaN on Si (cost advantages and wafer scaling) — each with tradeoffs relevant to MMIC vs. discrete implementations. Industry white papers from leading suppliers summarize the material/package trade space and practical design guidance for GaN on SiC devices used in RF amplifiers..

B. PA topologies and efficiency advances

High-efficiency PA classes (E, F, Doherty, envelope tracking, and hybrid harmonic-tuned variants) have been demonstrated with GaN, exploiting the device's ability to handle large voltage swings and harmonically-rich waveforms. Recent research has extended Class-E methods into broadband and linearized variants (multi-harmonic resonance, continuous class-E modes, and internally harmonic matched PAs) demonstrating PAE in the 60–80% range for various frequency bands and power levels. Importantly, mmWave and X/Ku-band GaN MMICs have reported high output powers and multi-watt PAs suitable for radar and satcom, showing GaN's viability across frequencies up to W-band in specialized processes.

C. Reliability, thermal, and nonlinear behavior

Despite performance advantages, GaN HEMTs present reliability challenges: trapping effects, current collapse, and degradation under high electric fields and temperature cycles. Recent comprehensive reviews discuss nonlinear mechanisms (gate leakage, trapping), modeling approaches, and reliability improvements (passivation, field-plate designs, and improved epitaxy). Thermal design—substrate selection (SiC), heat-spreading, and package thermal resistance—remains crucial for realizing simulated performance in hardware and for long-term device lifetime.

D. Market & system trends

Market analyses indicate increasing adoption of RF GaN across defense, 5G infrastructure, and satellite communications, with GaN on Si growth accelerating due to wafer scaling economics. Recent industry and strategy reports emphasize GaN's market momentum and the push from vendors to make GaN more accessible for commercial base stations and high-power modules.

Gap analysis. While many papers demonstrate device-level and discrete PA achievements, fewer open publications cover full chip-level (tape-out ready) co-design with layout, DRC/LVS concerns, and a validated path from harmonic-balance simulation to packaged prototype at sub-1 GHz. This gap motivates the current design emphasis on layout, thermal planning, and test strategy combined with state-of-the-art nonlinear simulation.

Table 1: Comparative Analysis of Key Performance Parameters: Existing Technologies (Si/GaAs) versus Gallium Nitride (GaN).

Parameter	Existing System (Si/GaAs)	Gap Identified	GaN Advantage
Efficiency	40–60%	Requirement >70%	Up to 78%
Frequency Range	Narrowband	Broadband operation required	Multi-band capability
Thermal Stability	Limited	High robustness needed	Wide bandgap, high thermal limits
Power Density	<2 W/mm	Requirement >10 W/mm	10–15 W/mm
SWaP Optimization	Bulky modules	Compact design required	Achievable with GaN HEMTs

IV. DESIGN OBJECTIVES & SPECIFICATIONS

This section lists design targets and constraints used throughout the project.

Primary objectives.

Target frequency: 900 MHz (primary), extendable to 1 GHz; appendix notes for S-band adaptation.

Small-signal gain: ≥ 20 dB (target $\approx 25\text{--}30$ dB in simulation).

Saturated output power (P_{1dB} / P_{sat}): $\geq +35$ dBm ($\geq \sim 3$ W) for MMIC; simulation goals indicated ~ 41 dBm (~ 12.9 W) under idealized large-signal drive (this corresponds to a discrete/device-level PA or multi-finger device).

PAE: $\geq 60\text{--}70\%$ target; simulation demonstrates $>80\%$ under optimized Class-E conditions (note: lab measurements typically show reduced PAE due to package and measurement losses).

Input/output impedance: $50\ \Omega$ system standard.

Stability: unconditional ($\mu > 1$) across intended bandwidth.

Linearity: IP_3 and adjacent channel metrics depend on application; for radar high linearity is less critical than efficiency, while for communications linearity tradeoffs may involve digital pre-distortion strategies.

Constraints and assumptions.

Simulations use vendor nonlinear models (or equivalent behavioral large-signal models) with idealized thermal boundary conditions; measured hardware results require conservative derating for packaging and substrate thermal impedance. Vendor application notes and white papers inform realistic conversion from simulated transmission-line lengths to physical microstrip dimensions and package effects.

Table 2: Key Simulation and Operating Parameters for the Class E Power Amplifier Design.

Input Parameter	Value in Simulation	Purpose
Center Frequency	1.0 GHz	The fundamental frequency of operation for the amplifier.
Input Power (P_{in})	35.25 dBm (~ 3.35 Watts)	The drive level for large-signal analysis, pushing the amplifier into its high-efficiency region.
Drain Voltage (V_{DRAIN})	+30.0 V	The main DC power source for the GaN transistor.
Gate Voltage (V_{GATE})	-3.6 V	The DC bias voltage used to set the transistor's quiescent operating point.
Source/Load Impedance	50 Ohms	The standard characteristic impedance for the test environment

V. METHODOLOGY & DESIGN FLOW

A. Device selection & modeling

Choose a GaN HEMT whose DC and RF characteristics meet voltage and current requirements. For sub-1 GHz high-power amplifiers designers often choose GaN on SiC devices (e.g., Wolfspeed family or comparable parts) for superior thermal dissipation. Obtain or create a nonlinear large-signal model (foundry or vendor X-parameter / VB-HB model) for harmonic-balance simulation.

Model validation. Validate the device model against vendor S-parameters and pulsed I-V data. If model-to-device mismatch is apparent, create a “translation table” that maps simulated transmission line lengths and widths to fabricated microstrip geometries using the intended substrate stack and dielectric properties.

B. Thermal management

GaN’s advantage is partly thermal, but thermal design is nontrivial: use SiC substrates or low thermal resistance packaging, consider heat spreaders, and model thermal impedance across die to package. Thermal simulations should estimate junction temperature under worst-case (continuous wave and pulsed duty cycle), and a margin for degradation and lifetime (MTTF) analysis should be included. Practical thermal management often uses thermal vias under die pads, metalized package bases, and dedicated heat sinks.

VI. CONCLUSION

This paper presented a comprehensive GaN RF PA design methodology, demonstrated strong simulated performance for a Class-E GaN amplifier with >80% simulated PAE and multi-watt output at ~1 GHz, and discussed thermal, packaging, and reliability considerations relevant to chip/tape-out and prototyping. GaN technology’s material advantages make it the technology of choice for modern high-power RF systems; however, closing the gap between simulation and measured hardware requires rigorous EM co-simulation, conservative thermal budgeting, and careful packaging considerations

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